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Core model of the electronics domain

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CONTENTS

FOREWORD.....	5
INTRODUCTION.....	7
1 Scope and object.....	8
2 Reference documents.....	9
3 General modelling issues	9
3.1 Ownership and reference	9
3.2 Uniqueness by value	12
3.3 Default values	12
3.4 Optional versus empty sets	12
3.5 Model topology.....	12
4 Concepts.....	13
4.1 The information base.....	13
4.2 Global ports and global port bundles	13
4.3 Libraries.....	13
4.4 Cells.....	14
4.5 Clusters and cell representation sets.....	14
4.6 Cell representations	14
4.7 Master ports and master port bundles	14
4.8 Instances	15
4.9 Instance ports and instance port bundles	15
5 Connectivity	16
5.1 Logical connectivity.....	16
5.2 Structural connectivity with wide instances	17
5.3 Structural connectivity of connectivity views	19
6 The design hierarchy mechanism	21
6.1 The design hierarchy.....	21
6.2 Annotations	23
7 Core Model for electronic design	24
7.1 Libraries.....	24
7.2 Interfacing to cells.....	25
7.3 Cell definition hierarchies	27
7.4 Instantiation	27
7.5 Logical connectivity.....	28
7.6 Structural connectivity.....	28
7.7 Global connectivity.....	32
7.8 Design and configuration.....	33
7.9 Annotation.....	34
8 Core Model EXPRESS-G.....	34
8.1 Partial EXPRESS-G of cell	35
8.2 Partial EXPRESS-G of cell_representation	36
8.3 Partial EXPRESS-G of cluster	37
8.4 Partial EXPRESS-G of cluster_configuration	38
8.5 Partial EXPRESS-G of cluster_interface	39
8.6 Partial EXPRESS-G of connectivity_generic_bus	40

8.7	Partial EXPRESS-G of connectivity_generic_net	41
8.8	Partial EXPRESS-G of design	42
8.9	Partial EXPRESS-G of global_port	43
8.10	Partial EXPRESS-G of information_base	44
8.11	Partial EXPRESS-G of instance.....	45
8.12	Partial EXPRESS-G of instance_configuration.....	46
8.13	Partial EXPRESS-G of library.....	47
8.14	Partial EXPRESS-G of master_port_annotate.....	48
8.15	Partial EXPRESS-G of name_information.....	49
8.16	Partial EXPRESS-G of occurrence_annotate	50
8.17	Partial EXPRESS-G of occurrence_annotate	51
8.18	Partial EXPRESS-G of occurrence_annotate	52
8.19	Partial EXPRESS-G of occurrence_hierarchy_annotate.....	53
8.20	Partial EXPRESS-G of port_structure	54
8.21	Partial EXPRESS-G of property.....	55
8.22	Partial EXPRESS-G of property_override	56
8.23	Partial EXPRESS-G of signal	57
9	Core Model schemas.....	58
9.1	connectivity_structure_model	58
9.2	connectivity_view_model	59
9.3	design_hierarchy_model.....	60
9.4	design_management_model	62
9.5	documentation_model	63
9.6	hierarchy_model.....	64
9.7	information_base_model	67
9.8	library_model	68
9.9	logical_connectivity_model.....	69
9.10	support_definition_model	70
10	Core Model information model	72
10.1	connectivity_structure_model	72
10.2	design_hierarchy_model.....	89
10.3	documentation_model	114
10.4	hierarchy_model.....	116
10.5	information_base_model	157
10.6	support_definition_model	166
11	Index	188
	Figure 1 – The owner relationship.....	10
	Figure 2 – Owner relationship with multiple potential owners	11
	Figure 3 – The reference mechanism	11
	Figure 4 – Uniqueness by value.....	12
	Figure 5 – An example of signal hierarchy	17
	Figure 6 – A net joins a port on an instance in the commoned style	18
	Figure 7 – A bus joins a port bundle on an instance in the commoned style	18
	Figure 8 – A bus joins a port bundle on an instance in the fanned-out style	19
	Figure 9 – Internal and external libraries.....	25
	Figure 10 – Port bundling – 1.....	26

Figure 11 – Port bundling – 2.....	26
Figure 12 – Instantiation	27
Figure 13 – Connectivity net	28
Figure 14 – Connectivity bus.....	29
Figure 15 – Connectivity bus – Commoning	29
Figure 16 – Connectivity bus – Logical equivalent of commoning	30
Figure 17 – Connectivity bus – Fanning-out	30
Figure 18 – Connectivity bus – Logical equivalent of fanning-out	31
Figure 19 – Connectivity bus-slice	31
Figure 20 – Connectivity ripper	32
Figure 21 – Global port scoping	33

INTERNATIONAL ELECTROTECHNICAL COMMISSION

CORE MODEL OF THE ELECTRONICS DOMAIN

FOREWORD

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The text of this standard is based on the following documents:

FDIS	Report on voting
93/172/FDIS	93/176/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

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This standard does not follow the rules for the structure of International Standards given in the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until 2012-07. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

INTRODUCTION

The Core Model of the electronics domain provides a common basis for design information handled by CAD systems within the electronic domain. It is the purpose of this model to provide a conceptual representation of the electronics domain, so that the compliant CAD systems handle a similar set of concepts, thus making inter-communication, sharing and exchange of design information a much easier task. It is not the purpose of this model to describe implementation details or to provide a data representation of electronics domain information.

The Core Model of the electronics domain, Edition 1.0, is referred to as the “Core Model” throughout this document. The Core Model, in part, has been created by enhancing the industry connectivity consensus model, EDIF CFI DR Alignment Model Version 1.0 (www.edif.org).

The chosen description language for this Core Model is EXPRESS, as defined by ISO 10303-11.

It is necessary to describe the Core Model as an information model in order to provide a formal definition of the design information that shall be recognized by the compliant CAD systems. The benefits of a formal description derive from its ability to provide an unambiguous representation of concepts, attributes and relationships, and the global rules and constraints that may be applied. By having such a description, it is possible to check the consistency and the correctness of the model as well as to provide a reliable starting-point for further development. It also facilitates the design of correct electronics CAD implementations based on this Core Model, as the actual implementation methods can be checked against the model.

This Core Model includes connectivity, hierarchy and design information for the electronics domain. Future parts of this Core Model standard may be extended to include other categories of information (for example, *cell_representation*, schematic representation, the PCB domain, symbols and display information).

In order to facilitate the creation of other parts of this Core Model standard, some objects have been used in this Core Model to facilitate support for other parts of the electronics domain. There are two types of such objects.

- Entities, such as *cell_representation*, are important concepts that provide support for defining other Core Model parts.
- Constraints: Some of constraints of this Core Model use conditions that are always true. They have been written in this way in order to ensure that they remain valid when the model is extended.

CORE MODEL OF THE ELECTRONICS DOMAIN

1 Scope and object

This International Standard provides the semantics definitions for the following categories of information related to electronic circuit designs. Each category of design information is modelled as an EXPRESS schema.

The Core Model consists of 10 schemas. Each of them is presented in this document as a separate chapter. At the beginning of each chapter, a description of the corresponding schema is provided.

- The *hierarchy_model* schema describes the hierarchical information of a cell, i.e. the way a cell may be divided into other cells.

A circuit may be divided into cells which, in turn, may be further subdivided into other cells, thus creating a hierarchy. The hierarchy information describes the cells, the possible cell representations and their instances.

- The *design_hierarchy_model* schema describes the annotation on an occurrence hierarchy.

The definition of a design requires that specific representations (views) of design objects in the hierarchy are selected. This unambiguously creates a configured design hierarchy. This concept is similar to the configuration of a design in VHDL and is related to view selection mechanisms of other electronics design domain information models in industry. The design hierarchy identifies top-level design cells and may provide annotated design-specific data into the elaborated hierarchy.

- The *connectivity_view_model* schema describes the connectivity information of a cell.

This describes the way in which the circuits are connected in order that information or energy may flow from one part of a design or product to another. The Core Model subdivides this information into

- the *logical_connectivity_model* schema which describes the connectivity for a given level of a hierarchy.

Logical connectivity information describes the bit level, abstract electrical connectivity for a given level of a hierarchy, in terms of signals and signal groups.

- the *connectivity_structure_model* schema which describes the structural connectivity of a connectivity view.

Structural connectivity information describes the connectivity, for a given level of a hierarchy, from the structural point of view. The structural connectivity is specified in terms of busses, nets and rippers. Such a structural representation is used to provide support for physical implementation and annotation.

- The *library_model* schema describes the technology information contained in a library, as well as the reusable objects and data.

A library provides a means of grouping cell definitions. A library may be used to group other classes of reusable objects and information as well. Information in a library may be related in terms of technology information.

- The *information_base_model* schema describes the information in an information base.

The *information_base* describes the kind of information that can be found directly in an information base.

In addition, the following information is also included in the model.

- The *design_management_model* schema provides the design management information. This information is needed to trace back to the source or the owner of the data.
- The *documentation_model* schema describes the documentation provided for an object.
- The *support_definition_model* schema contains the definition of some auxiliary entities, types and functions that are used by several schemas.

Names of objects used in this Core Model standard were chosen to be the same as the names of the similar objects and concepts in existing electronics domain information models wherever possible.

2 Reference documents

IEC 61690-1:2000, *Electronic design interchange format (EDIF) – Part 1: Version 300*

IEC 61690-2:2000, *Electronic design interchange format (EDIF) – Part 2: Version 400*

ISO 13030-11:1994, *Industrial automation systems and integration – Product representation and exchange – Part 11: Description methods: The EXPRESS-I language reference manual*