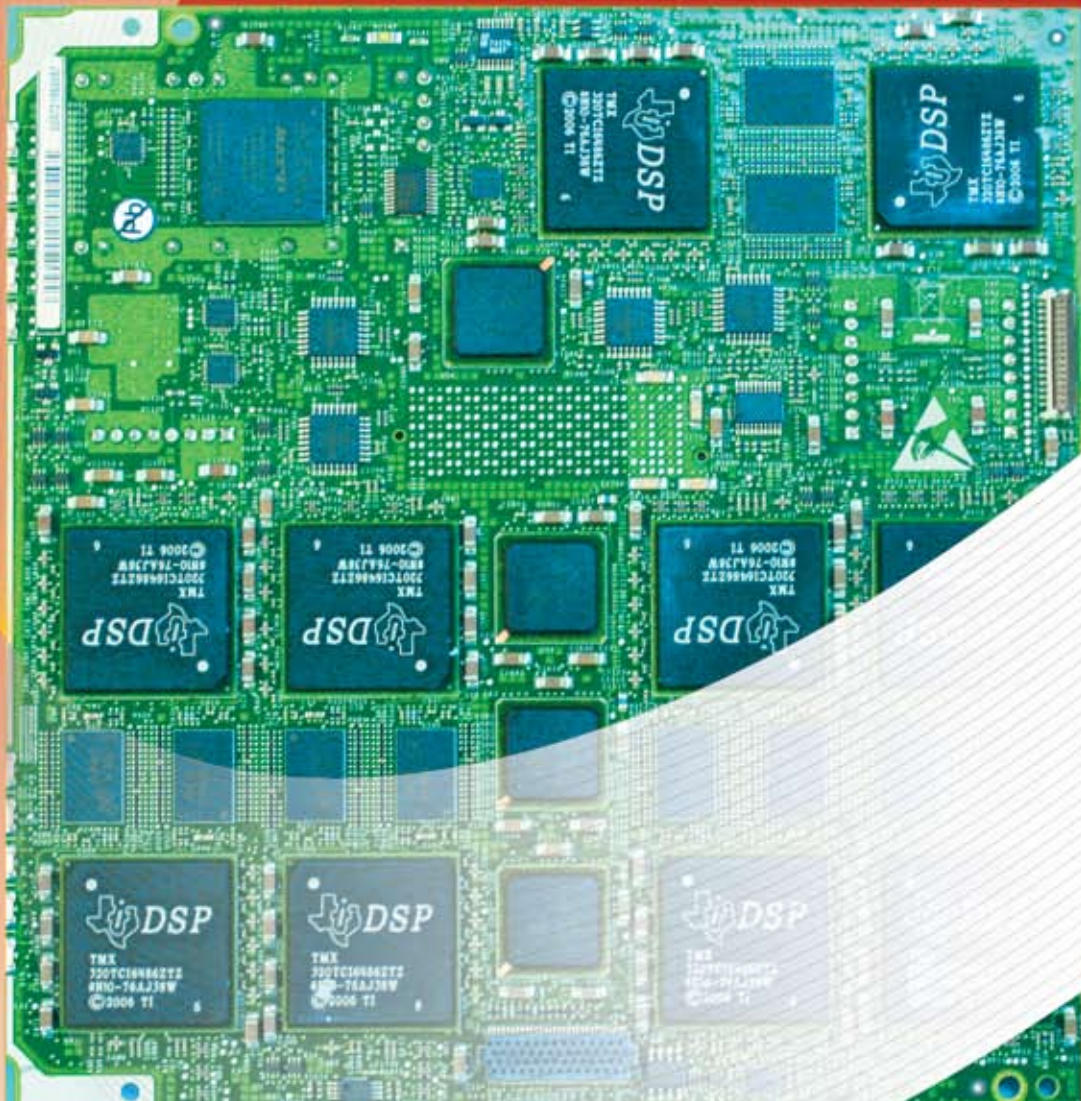


IPC-7095B

Design and Assembly Process Implementation for BGAs

March 2008



Association Connecting Electronics Industries



The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee (TAEC) adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

Notice

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

IPC Position Statement on Specification Revision Change

It is the position of IPC's Technical Activities Executive Committee that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC publication is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision. Adopted October 6, 1998

Why is there a charge for this document?

Your purchase of this document contributes to the ongoing development of new and updated industry standards and publications. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards and publications development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low to allow as many companies as possible to participate. Therefore, the standards and publications revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards and publications, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit www.ipc.org or call 847/597-2872.

Thank you for your continued support.



IPC-7095B

Design and Assembly Process Implementation for BGAs

Developed by the Device Manufacturers Interface
Committee of IPC

Supersedes:

IPC-7095A - October 2004

IPC-7095 - August 2000

Users of this publication are encouraged to participate in the
development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, Illinois
60015-1249
Tel 847 615.7100
Fax 847 615.7105

This Page Intentionally Left Blank

Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the IPC Ball Grid Array Task Group (5-21f) of the Assembly & Joining Processes Committee (5-20) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

Assembly & Joining Processes Committee

Chair
Leo P. Lambert
EPTAC Corporation

Vice Chair
Renee J. Michalkiewicz
Trace Laboratories - East

Ball Grid Array Task Group

Chair
Ray Prasad
Ray Prasad Consultancy Group

Technical Liaisons of the IPC Board of Directors

Peter Bigelow
IMI Inc.

Sammy Yi
Flextronics International

Ball Grid Array Task Group

David Adams, Rockwell Collins
Syed Ahmad, NDSU
Dudi Amir, Intel Corporation
Raiyomand Aspandiar, Intel Corporation
David Brown, Lockheed Martin Aeronautics
Lyle Burhenn, BAE Systems
Scott Buttars, Intel Corporation
Beverley Christian, Research in Motion Ltd.
Geoffrey Dick, Lockheed Martin
Allen Donaldson, Intel Corporation
Don Dupriest, Lockheed Martin Missiles and Fire Control
Werner Engelmaier, Engelmaier Associates
Gary Ferrari, FTG Circuits
Joe Fjelstad, SiliconPipe Inc.
Lionel Fullwood, WKK Distribution
Mahendra Gandhi, Northrop Grumman Space Technology
Hue Green, Lockheed Martin Space Systems
Mike Green, Lockheed Martin Space Systems

Constantin Hudon, Varitron Technologies
Greg Hurst, BAE Systems
Glen Leinbach, Agilent Technologies
Paul Lotosky, Cookson Electronics
Helen Lowe, Celestica
Robert Mazium, Phoenix/X-Ray
Karen McConnell, Lockheed Martin EPICenter
George Milad, Uyemura In'l Corporation
Jim Moffit, Moffit Consulting Services
Barry Morris, Advanced Rework Technology
George Oxx, Flextronics Technology Inc.
Deepak Pai, General Dynamics Adv Info Sys
Mel Parrish, Soldering Technology International
Sam Polk, Lockheed Martin Missiles and Fire Control
Ray Prasad, Ray Prasad Consultancy Group
Guy Ramsey, R&D Assembly
Teresa Rowe, AAI Corporation

Robert Rowland, RadiSys
Jim Rudig, Intel Corporation
Waleed Rusheidat, Jabil Circuit
Marty Scionti, Raytheon Missile Systems
Gregory Servis, Lockheed Martin
Vern Solberg, Solberg Technical Consulting
Kerry Spencer, Lockheed Martin Missile & Fire Control
Dung Tiet, Lockheed Martin Space Systems
Neil Trelford, Nortel
Kris Troxel, Hewlett Packard
Dave Vanacek, Lockheed Martin Aeronautics
Sharon Ventress, U.S. Army Aviation & Missile
Rob Walls, PIEK
Dewey Whittaker, Honeywell Aerospace
Linda Woody, Lockheed Martin
Fonda Wu, Raytheon Electronics Systems
Michael Yuen, Microsoft Corp.
Gil Zweig, Glenbrook Technologies

A special note of thanks goes to the following individuals for their dedication to bringing this project to fruition. We would like to highlight those individuals who made major contributions to the development of this standard.

Dudi Amir, Intel Corporation

Raiyomand Aspandiar, Intel Corporation

Scott Buttars, Intel Corporation

Werner Engelmaier, Engelmaier Associates

Mike Green, Lockheed Martin Space Systems

Helen Lowe, Celestica

Karen McConnell, Lockheed Martin EPICenter

Ray Prasad, Ray Prasad Consultancy Group

Robert Rowland, RadiSys

Vern Solberg, Solberg Technical Consulting

Kris Troxel, Hewlett Packard

Front and back cover photos courtesy of RadiSys Corporation

Table of Contents

1 SCOPE	1	4.3.1 Industry Standards for BGA	16
1.1 Purpose	1	4.3.2 Ball Pitch	17
1.2 Intent	1	4.3.3 BGA Package Outline	18
2 APPLICABLE DOCUMENTS	1	4.3.4 Ball Size Relationships	19
2.1 IPC	1	4.3.5 Coplanarity	19
2.2 JEDEC	1	4.4 Component Packaging Style Considerations	19
3 SELECTION CRITERIA AND MANAGING BGA IMPLEMENTATION	2	4.4.1 Solder Ball Alloy	20
3.1 Description of Infrastructure	3	4.4.2 Ball Attach Process	20
3.1.1 Land Patterns and Circuit Board Considerations	3	4.4.3 Ceramic Ball Grid Array	21
3.1.2 Technology Comparison	5	4.4.4 Ceramic Column Grid Arrays	21
3.1.3 Assembly Equipment Impact	7	4.4.5 Tape Ball Grid Arrays	22
3.1.4 Stencil Requirements	7	4.4.6 Multiple Die Packaging	22
3.1.5 Inspection Requirements	8	4.4.7 System-in-Package (SiP)	23
3.1.6 Test	8	4.4.8 3D Folded Package Technology	23
3.2 Time-to-Market Readiness	8	4.4.9 Ball Stack, Package-on-Package	23
3.3 Methodology	9	4.4.10 Folded and Stacked Packaging Combination ...	24
3.4 Process Step Analysis	9	4.4.11 Benefits of Multiple Die Packaging	24
3.5 BGA Limitations and Issues	9	4.5 BGA Connectors	24
3.5.1 Visual Inspection	9	4.5.1 Material Considerations for BGA Connectors ..	24
3.5.2 Moisture Sensitivity	9	4.5.2 Attachment Considerations for BGA Connectors	25
3.5.3 Thermally Unbalanced BGA Design	10	4.6 BGA Construction Materials	25
3.5.4 Rework	10	4.6.1 Types of Substrate Materials	25
3.5.5 Cost	11	4.6.2 Properties of Substrate Materials	26
3.5.6 Availability	12	4.7 BGA Package Design Considerations	27
3.5.7 Voids in BGA	12	4.7.1 Power and Ground Planes	27
3.5.8 Standardization Issues	12	4.7.2 Signal Integrity	28
3.5.9 Reliability Concerns	12	4.7.3 Heat Spreader Incorporation Inside the Package	28
4 COMPONENT CONSIDERATIONS	12	4.8 BGA Package Acceptance Criteria and Shipping Format	28
4.1 Component Packaging Comparisons and Drivers	12	4.8.1 Missing Balls	28
4.1.1 Package Feature Comparisons	12	4.8.2 Voids in Solder Balls	28
4.1.2 BGA Package Drivers	13	4.8.3 Solder Ball Attach Integrity	29
4.1.3 Cost Issues	13	4.8.4 Package Coplanarity	29
4.1.4 Component Handling	13	4.8.5 Moisture Sensitivity (Baking, Storage, Handling, Rebaking)	30
4.1.5 Thermal Performance	13	4.8.6 Shipping Medium (Tape and Reel, Trays, Tubes)	30
4.1.6 Real Estate	13	4.8.7 Solder Ball Alloy	31
4.1.7 Electrical Performance	14	5 PCBs AND OTHER MOUNTING STRUCTURES ..	31
4.2 Die Mounting in the BGA Package	14	5.1 Types of Mounting Structures	31
4.2.1 Wire Bond	14	5.1.1 Organic Resin Systems	31
4.2.2 Flip Chip	15	5.1.2 Inorganic Structures	31
4.3 Standardization	16		

5.1.3	Layering (Multilayer, Sequential or Build-Up)	31	6.4	Impact of Wave Solder on Top Side BGAs	57
5.2	Properties of Mounting Structures	31	6.4.1	Top Side Reflow	57
5.2.1	Resin Systems	31	6.4.2	Impact of Top Side Reflow	57
5.2.2	Reinforcements	33	6.4.3	Methods of Avoiding Top Side Reflow	58
5.2.3	Laminate Material Properties	33	6.4.4	Top Side Reflow for Lead-Free Boards	59
5.2.4	Reliability Concerns with High Lead-Free Soldering Temperatures	33	6.5	Testability and Test Point Access	59
5.2.5	Thermal Expansion	33	6.5.1	Component Testing	59
5.2.6	Glass Transition Temperature	33	6.5.2	Damage to the Solder Balls During Test and Burn-In	60
5.2.7	Moisture Absorption	34	6.5.3	Bare Board Testing	61
5.3	Surface Finishes	34	6.5.4	Assembly Testing	61
5.3.1	Hot Air Solder Leveling (HASL)	34	6.6	Other Design for Manufacturability Issues	64
5.3.2	Organic Surface Protection (Organic Solderability Preservative) OSP Coatings	37	6.6.1	Panel/Subpanel Design	64
5.3.3	Noble Platings/Coatings	37	6.6.2	In-Process/End Product Test Coupons	64
5.4	Solder Mask	40	6.7	Thermal Management	65
5.4.1	Wet and Dry Film Solder Masks	41	6.7.1	Conduction	65
5.4.2	Photoimageable Solder Masks	41	6.7.2	Radiation	66
5.4.3	Registration	42	6.7.3	Convection	67
5.4.4	Via Protection	42	6.7.4	Thermal Interface Materials	67
5.5	Thermal Spreader Structure Incorporation (e.g., Metal Core Boards)	44	6.7.5	Heat Sink Attachment Methods for BGAs	67
5.5.1	Lamination Sequences	44	6.8	Documentation and Electronic Data Transfer ...	69
5.5.2	Heat Transfer Pathway	44	6.8.1	Drawing Requirements	69
6	PRINTED CIRCUIT ASSEMBLY DESIGN CONSIDERATION	46	6.8.2	Equipment Messaging Protocols	70
6.1	Component Placement and Clearances	46	6.8.3	Specifications	71
6.1.1	Pick and Place Requirements	46	7	ASSEMBLY OF BGAS ON PRINTED CIRCUIT BOARDS	71
6.1.2	Repair/Rework Requirements	46	7.1	SMT Assembly Processes	71
6.1.3	Global Placement	47	7.1.1	Solder Paste and Its Application	71
6.1.4	Alignment Legends (Silkscreen, Copper Features, Pin 1 Identifier)	47	7.1.2	Component Placement Impact	73
6.2	Attachment Sites (Land Patterns and Vias)	48	7.1.3	Vision Systems for Placement	73
6.2.1	Big vs. Small Land and Impact on Routing	48	7.1.4	Reflow Soldering and Profiling	74
6.2.2	Solder Mask vs. Metal Defined Land Design ..	48	7.1.5	Material Issues	78
6.2.3	Conductor Width	50	7.1.6	Vapor Phase	78
6.2.4	Via Size and Location	50	7.1.7	Cleaning vs. No-Clean	79
6.3	Escape and Conductor Routing Strategies	51	7.1.8	Package Standoff	79
6.3.1	Escape Strategies	53	7.2	Post-SMT Processes	80
6.3.2	Surface Conductor Details	54	7.2.1	Conformal Coatings	80
6.3.3	Dog Bone Through Via Details	54	7.2.2	Use of Underfills and Adhesives	81
6.3.4	Design for Mechanical Strain	54	7.2.3	Depaneling of Boards and Modules	84
6.3.5	Uncapped Via-in-Pad and Impact on Reliability Issues	55	7.3	Inspection Techniques	84
6.3.6	Fine Pitch BGA Microvia in Pad Strategies	56	7.3.1	X-Ray Usage	84
6.3.7	Power and Ground Connectivity	57	7.3.2	X-Ray Image Acquisition	85
			7.3.3	Definition and Discussion of X-Ray System Terminology	86
			7.3.4	Analysis of the X-Ray Image	88
			7.3.5	Scanning Acoustic Microscopy	90

7.3.6	BGA Standoff Measurement	90	8.5.4	Reliability of Solder Attachments of Ceramic Grid Array	121
7.3.7	Optical Inspection	90	8.5.5	Lead-Free Soldering of BGAs	121
7.3.8	Destructive Analysis Methods	92	8.6	Design for Reliability (DfR) Process	127
7.4	Testing and Product Verification	93	8.7	Validation and Qualification Tests	128
7.4.1	Electrical Testing	93	8.8	Screening Procedures	128
7.4.2	Test Coverage	94	8.8.1	Solder Joint Defects	128
7.4.3	Burn-In Testing	94	8.8.2	Screening Recommendations	128
7.4.4	Product Screening Tests	94			
7.5	Assembly Process Control Criteria for Plastic BGAs	94	9	DEFECT AND FAILURE ANALYSIS	
7.5.1	Voids	95		CASE STUDIES	129
7.5.2	Solder Bridging	106	9.1	Solder Mask Defined BGA Conditions	129
7.5.3	Opens	106	9.1.1	Solder Mask Defined and Nondefined Lands ..	129
7.5.4	Cold Solder	106	9.1.2	Solder Mask Defined Land on Product Board	129
7.5.5	Defect Correlation/Process Improvement	106	9.1.3	Solder Mask Defined BGA Failures	130
7.5.6	Insufficient/Uneven Heating	107	9.2	Over-Collapse BGA Solder Ball Conditions ..	130
7.5.7	Component Defects	107	9.2.1	BGA Ball Shape without Heat Slug 500 µm Standoff Height	130
7.6	Repair Processes	108	9.2.2	BGA Ball Shape with Heat Slug 375 µm Standoff Height	130
7.6.1	Rework/Repair Philosophy	108	9.2.3	BGA Ball Shape with Heat Slug 300 µm Standoff Height	131
7.6.2	Removal of BGA	108	9.2.4	Critical Solder Paste Conditions	131
7.6.3	Replacement	109	9.2.5	Thicker Paste Deposit	131
8	RELIABILITY	111	9.2.6	Void Determination Through X-Ray and Cross-Section	131
8.1	Accelerated Reliability Testing	111	9.2.7	Voids and Uneven Solder Balls	132
8.2	Damage Mechanisms and Failure of Solder Attachments	112	9.2.8	Eggshell Void	132
8.2.1	Comparison of Thermal Fatigue Crack Growth Mechanism in SAC vs. Tin/ Lead BGA Solder Joints	113	9.3	BGA Interposer Bow and Twist	132
8.2.2	Mixed Alloy Soldering	113	9.3.1	BGA Interposer Warp	133
8.3	Solder Joints and Attachment Types	115	9.3.2	Solder Joint Opens Due to Interposer Warp ...	133
8.3.1	Global Expansion Mismatch	116	9.4	Solder Joint Conditions	133
8.3.2	Local Expansion Mismatch	116	9.4.1	Target Solder Condition	134
8.3.3	Internal Expansion Mismatch	116	9.4.2	Solder Balls With Excessive Oxide	134
8.4	Solder Attachment Failure	116	9.4.3	Evidence of Dewetting	134
8.4.1	Solder Attachment Failure Classification	116	9.4.4	Mottled Condition	134
8.4.2	Failure Signature-1: Cold Solder	117	9.4.5	Tin/lead Solder Ball Evaluation	135
8.4.3	Failure Signature-2: Land, Nonsolderable	117	9.4.6	SAC Alloy	135
8.4.4	Failure Signature-3: Ball Drop	117	9.4.7	Cold Solder Joint	135
8.4.5	Failure Signature-4: Missing Ball	118	9.4.8	Incomplete Joining Due to Land Contamination	135
8.4.6	Failure Signature-5: Package Warpage	118	9.4.9	Deformed Solder Ball Contamination	136
8.4.7	Failure Signature-6: Mechanical Failure	118	9.4.10	Deformed Solder Ball	136
8.4.8	Failure Signature-7: Insufficient Reflow	119	9.4.11	Insufficient Solder and Flux for Proper Joint Formation	136
8.5	Critical Factors to Impact Reliability	119	9.4.12	Reduced Termination Contact Area	136
8.5.1	Package Technology	119	9.4.13	Excessive Solder Bridging	137
8.5.2	Stand-off Height	120	9.4.14	Incomplete Solder Reflow	137
8.5.3	PCB Design Considerations	121			

9.4.15	Disturbed Solder Joint	137
9.4.16	Missing Solder	137
10	GLOSSARY AND ACRONYMS	138
11	BIBLIOGRAPHY AND REFERENCES	139

Figures

Figure 3-1	BGA package manufacturing process	2	Figure 4-18	BGA connector	25
Figure 3-2	Area array I/O position comparisons	4	Figure 4-19	Example of missing balls on a BGA component	28
Figure 3-3	Area array I/O position patterns	5	Figure 4-20	Example of voids in eutectic solder balls at incoming inspection	29
Figure 3-4	MCM type 2S-L-WB	5	Figure 4-21	Examples of solder ball/land surface conditions	29
Figure 3-5	Conductor width to pitch relationship	7	Figure 4-22	Establishing BGA coplanarity requirement	30
Figure 3-6	Plastic ball grid array, chip wire bonded	8	Figure 4-23	Ball contact positional tolerance	30
Figure 3-7	Ball grid array, flip chip bonded	8	Figure 5-1	Examples of different build-up constructions	32
Figure 3-8	BGA warpage	11	Figure 5-2	Expansion rate above T_g	34
Figure 4-1	Partial area under the die is used to provide ground for the die. The rest of the area has been used for signal routing but has been covered with solder mask to isolate it from the conductive adhesive under the die.	14	Figure 5-3	Hot air solder level (HASL) surface topology comparison	36
Figure 4-2	Use of glass die to optimize the adhesive dispensing process for void-free controlled fill and squeeze-out. The picture on the top shows the adhesive dispense pattern on the die site. The picture on the bottom shows the placed glass die to view voids and filling characteristics. The adhesive provides full die coverage for attachment but partial coverage to ground through a smaller than die ground pad, allowing a larger portion of the area under the die for signal routing saving valuable real estate and making the resulting package smaller.	15	Figure 5-4	Black pad related fracture showing crack between Nickel & Ni-Sn intermetallic layer	38
Figure 4-3	BOC BGA construction	15	Figure 5-5	Crack location for a) black pad related failure and (b) interfacial fracture when using ENIG surface finish	38
Figure 4-4	Top of molded BOC type BGA	16	Figure 5-6	Typical mud crack appearance of black pad Surface	39
Figure 4-5	Flip-chip (bumped die) on BGA substrate	16	Figure 5-7	A large region of severe black pad with corrosion spikes protruding into nickel rich layer through phosphorus rich layer underneath immersion gold surface	39
Figure 4-6	Plastic ball grid array (BGA) package	21	Figure 5-8	Graphic depiction of electroless nickel, electroless palladium/immersion gold	40
Figure 4-7	Cross-section of a ceramic ball grid array (CBGA) package	21	Figure 5-9	Graphic depiction of directed immersion gold	40
Figure 4-8	Ceramic ball grid array (CBGA) package	21	Figure 5-10	Work and turn panel layout	43
Figure 4-9	Cross-section of a ceramic column grid array (CCGA) package	21	Figure 5-11	Distance from tented land clearance	43
Figure 4-10	Polyimide film based lead-bond μ BGA package substrate furnishes close coupling between die pad and ball contact	22	Figure 5-12	Via plug methods	45
Figure 4-11	Comparing in-package circuit routing capability of the single metal layer tape substrate to two metal layer tape substrate ...	22	Figure 5-13	Solder filled and tented via blow-out	46
Figure 4-12	Single package die-stack BGA	23	Figure 5-14	Metal core board construction examples	46
Figure 4-13	Custom eight die (flip-chip and wire-bond) SiP assembly	23	Figure 6-1	BGA alignment marks	47
Figure 4-14	Folded multiple-die BGA package	23	Figure 6-2	Solder lands for BGA components	49
Figure 4-15	Package-on-package FBGA	24	Figure 6-3	Metal defined land attachment profile	49
Figure 4-16	SO-DIMM memory card assembly	24	Figure 6-4	Solder mask stress concentration	49
Figure 4-17	Folded and stacked multiple die BGA package	24	Figure 6-5	Solder joint geometry contrast	49
			Figure 6-6	Good/bad solder mask design	50
			Figure 6-7	Examples of metal-defined land	50
			Figure 6-8	Quadrant dog bone BGA pattern	51
			Figure 6-9	Square array	52
			Figure 6-10	Rectangular array	52
			Figure 6-11	Depopulated array	52
			Figure 6-12	Square array with missing balls	52
			Figure 6-13	Interspersed array	53
			Figure 6-14	Conductor routing strategy	53
			Figure 6-15	BGA dogbone land pattern preferred direction for conductor routing	55
			Figure 6-16	Preferred screw and support placement	55
			Figure 6-17	Connector screw support placement	55
			Figure 6-18	Cross section of 0.75 mm ball with via-in-pad structure (Indent to the upper left of the ball is an artifact.)	55

Figure 6-19	Cross section of via-in-pad design showing via cap and solder ball	55	Figure 7-12	Examples of underfill voids - small, medium and large; upper left, lower left and left of solder balls, respectively	82
Figure 6-20	Via-in-pad process descriptions	56	Figure 7-13	Example of partial underfill - package was pulled from the PCB and dark underfill can be seen in the corners	82
Figure 6-21	Microvia example	56	Figure 7-14	Corner applied adhesive	83
Figure 6-22	Microvia in pad voiding	57	Figure 7-15	Critical dimension for application of prereflow corner glue	83
Figure 6-23	Ground or power BGA connection	57	Figure 7-16	Typical corner glue failure mode in shock if glue area is too low - Solder mask rips off board and does not protect the solder joints	83
Figure 6-24	Example of top side reflow joints	57	Figure 7-17	Fundamentals of X-ray technology	85
Figure 6-25	Example of wave solder temperature profile of top-side of mixed component assembly	58	Figure 7-18	X-ray example of missing solder balls	85
Figure 6-26	Heat pathways to BGA solder joint during wave soldering	58	Figure 7-19	X-ray example of voiding in solder ball contacts	85
Figure 6-27	Methods of avoiding BGA topside solder joint reflow	59	Figure 7-20	Manual X-ray system image quality	86
Figure 6-28	An example of a side contact made with a tweezers type contact	60	Figure 7-21	Example of X-ray pin cushion distortion and voltage blooming	86
Figure 6-29	Pogo-pin type electrical contact impressions on the bottom of a solder ball	60	Figure 7-22	Transmission image (2D)	86
Figure 6-30	Area array land pattern testing	62	Figure 7-23	Tomosynthesis image (3D)	87
Figure 6-31	Board panelization	65	Figure 7-24	Laminographic cross-section image (3D)	87
Figure 6-32	Comb pattern examples	66	Figure 7-25	Transmission example	87
Figure 6-33	Heat sink attached to a BGA with an adhesive	68	Figure 7-26	Oblique viewing board tilt	88
Figure 6-34	Heat sink attached to a BGA with a clip that hooks onto the component substrate	68	Figure 7-27	Oblique viewing detector tilt	88
Figure 6-35	Heat sink attached to a BGA with a clip that hooks into a through-hole on the printed circuit board	68	Figure 7-28	Top down view of FBGA solder joints	88
Figure 6-36	Heat sink attached to a BGA with a clip that hooks onto a stake soldered in the printed circuit board	69	Figure 7-29	Oblique view of FBGA solder joints	88
Figure 6-37	Heat sink attached to a BGA by wave soldering its pins in a through-hole in the printed circuit board	69	Figure 7-30	Tomosynthesis	89
Figure 7-1	Aspect and area ratios for complete paste release	72	Figure 7-31	Scanned beam X-ray laminography	89
Figure 7-2	High lead and eutectic solder ball and joint comparison	73	Figure 7-32	Scanning acoustic microscopy	91
Figure 7-3	Example of peak reflow temperatures at various locations at or near a BGA	74	Figure 7-33	Endoscope example	91
Figure 7-4	Schematic of reflow profile for tin/lead assemblies	75	Figure 7-34	Lead-free 1.27 mm pitch BGA reflowed in nitrogen and washed between SMT passes	91
Figure 7-5	An example of tin/lead profile with multiple thermocouples	76	Figure 7-35	Lead-free BGA reflowed in air and washed between SMT passes	92
Figure 7-6	Schematic of reflow profile for lead-free assemblies	76	Figure 7-36	Engineering crack evaluation technique	93
Figure 7-7	Examples of lead-free profiles with soak (top) and ramp to peak (bottom) with multiple thermocouples. The profiles with soak tend to reduce voids in BGAs.	76	Figure 7-37	A solder ball cross sectioned through a void in the solder ball	93
Figure 7-8	Locations of thermocouples on a board with large and small components	77	Figure 7-38	Cross-section of a crack initiation at the ball/pad interface	93
Figure 7-9	Recommended locations of thermocouples on a BGA	77	Figure 7-39	No dye penetration under the ball	94
Figure 7-10	Effect of having solder mask relief around the BGA lands of the board	80	Figure 7-40	Corner balls have 80-100% dye penetration which indicate a crack	94
Figure 7-11	Flow of underfill between two parallel surfaces	82	Figure 7-41	Small voids clustered in mass at the ball-to-land interface	96
			Figure 7-42	X-ray image of solder balls with voids at 50 kV (a) and 60 kV (b)	97
			Figure 7-43	Typical size and location of various types of voids in a BGA solder joint	98
			Figure 7-44	Example of voided area at land and board Interface	98
			Figure 7-45	Typical flow diagram for void assessment ...	100

Table 6-10	Conductor routing - 0.8 mm Pitch	54	Table 7-10	Ball-to-void size image - comparison for various ball diameters	104
Table 6-11	Effects of material type on conduction	66	Table 7-11	C=0 sampling plan (sample size for specific index value*)	106
Table 6-12	Emissivity ratings for certain materials	66	Table 7-12	Repair process temperature profiles for tin lead assembly	111
Table 7-1	Particle size comparisons	72	Table 7-13	Repair process temperature profiles for lead-free assemblies	111
Table 7-2	Solder paste volume requirements for ceramic array packages	73	Table 8-1	Accelerated testing for end use environments	112
Table 7-3	Profile comparison between SnPb and SAC alloys	75	Table 8-2	Tin/lead component compatibility with lead-free reflow soldering	114
Table 7-4	Inspection usage application recommendations	84	Table 8-3	Typical stand-off heights for tin/lead balls (in mm)	120
Table 7-5	Field of view for inspection	90	Table 8-4	Common solders, their melting points, advantages and drawbacks	123
Table 7-6	Void classification	97	Table 8-5	Comparison of lead-free solder alloy compositions in the Sn-Ag-Cu family selection by various consortia	123
Table 7-7	Corrective action indicator for lands used with 1.5, 1.27 or 1.0 mm pitch	101	Table 8-6	Types of lead-free assemblies possible	125
Table 7-8	Corrective action indicator for lands used with 0.8, 0.65 or 0.5 mm pitch	102			
Table 7-9	Corrective action indicator for microvia in pad lands used with 0.5, 0.4 or 0.3 mm pitch	103			

This Page Intentionally Left Blank

Design and Assembly Process Implementation for BGAs

1 SCOPE

This document describes the design and assembly challenges for implementing Ball Grid Array (BGA) and Fine Pitch BGA (FBGA) technology. The effect of BGA and FBGA on current technology and component types are addressed, as is the move to lead-free assembly processes. The focus on the information contained herein is on critical inspection, repair, and reliability issues associated with BGAs. Throughout this document the word “BGA” can mean all types and forms of ball/column grid array packages.

1.1 Purpose The target audiences for this document are managers, design and process engineers, and operators and technicians who deal with the electronic assembly, inspection, and repair processes. The intent is to provide useful and practical information to those who are using BGAs, those who are considering BGA implementation and companies who are in the process of transition from the standard tin/lead reflow processes to those that use lead-free materials in the assembly of BGA type components.

1.2 Intent The new challenge in implementing BGA assembly processes, along with other types of components, is the need to meet the legislative directives that declare certain materials as hazardous to the environment. The requirements to eliminate these materials from electronic components have caused component manufacturers to rethink the materials used for encapsulation, the plating finishes on the components and the metal alloys used in the assembly attachment process.

This document, although not a complete recipe, identifies many of the characteristics that influence the successful implementation of a robust assembly process. In many applications, the variation between assembly methods and materials is reviewed with the intent to highlight significant differences that relate to the quality and reliability of the final product. The accept/reject criteria for BGA assemblies, used in contractual agreements, is established by J-STD-001 and IPC-A-610.

2 APPLICABLE DOCUMENTS

2.1 IPC¹

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

J-STD-020 Handling Requirements for Moisture Sensitive Components

J-STD-033 Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

IPC-T-50 Terms and Definitions for Printed Boards and Printed Board Assemblies

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-D-325 Documentation Requirements for Printed Boards

IPC-D-350 Printed Board Description in Digital Form

IPC-D-356 Bare Substrate Electrical Test Information in Digital Form

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Attachments

IPC-2221 Generic Standard on Printed Board Design

IPC-2511 Generic Requirements for Implementation of Product Manufacturing Description Data and Transfer

IPC-2581 Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology

IPC-7094 Design and Assembly Process Implementation for Flip Chip and Die Size Components

IPC-7351 Generic Requirements for Surface Mount Design and Land Pattern Standard

IPC-7525 Stencil Design Guidelines

IPC-7711/7721 Rework, Modification and Repair of Electronic Assemblies

IPC-9701 Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

IPC/JEDEC-9704 Printed Wiring Board Strain Gage Test Guideline

2.2 JEDEC²

JEP95 Section 4.5 Fine Pitch (Square) Ball Grid Array Package (FBGA)

1. www.ipc.org

2. www.jedec.org