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# ***JOINT INDUSTRY STANDARD***

Solderability  
Tests for  
Printed Boards



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IPC J-STD-003C

# Solderability Tests for Printed Boards

Developed by the Printed Circuit Board Solderability Specifications Task Group (5-23a) of the Assembly and Joining Committee (5-20) of IPC

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Contact:

**IPC**

3000 Lakeside Drive, Suite 309S  
Bannockburn, IL 60015-1249  
Phone ( 847) 615-7100  
Fax (847) 615-7105

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---

### Assembly and Joining Committee

Chair  
Leo P. Lambert  
EPTAC

Vice Chair  
Renee J. Michalkiewicz  
Trace Laboratories - Baltimore

### Printed Circuit Board Solderability Specifications Task Group

Chair  
Gerard A. Obrien  
Solderability Testing & Solutions, Inc.

Vice Chair  
Michah Pledger  
Pledger Consulting

### Technical Liaison of the IPC Board of Directors

Bob Neves  
Microtek Laboratories

---

### Printed Circuit Board Solderability Specifications Task Group

Douglas Schueller, AbelConn, LLC  
Constantino Gonzalez, ACME Training & Consulting  
Mitchell Holtzer, Alpha  
Anna Lifton, Alpha  
Karen Tellefsen, Alpha  
Andrew Giamis, Andrew Corporation  
George Wenger, Andrew Corporation  
Arnie Melby, Appareo Systems, LLC  
Greg Alexander, Ascentech LLC  
Fritz, Byle Astronautics Corp. of America  
Christopher, Ryder, AT&S Austria Technologie & Systemtechnik AG  
William Dieffenbacher, BAE Systems Platform Solutions  
Beverly Christian, BlackBerry  
Mary Bellon, Boeing Research & Development  
Todd MacFadden, Bose Corporation  
Louis Hart, Compunetics Inc.  
Israel Martinez, Continental Automotive Nogales S.A. de C.V.  
Mark Fulcher, Continental Automotive Systems  
Brian Madsen, Continental Automotive Systems  
David Corbett, Defense Supply Center Columbus  
Lowell Sherman, Defense Supply Center Columbus  
Glenn Dody, Dody Consulting  
Anne Lomonte, Draeger Medical Systems, Inc.

Peter Bratin, ECI Technology, Inc.  
Michael Pavlov, ECI Technology, Inc.  
Julie Filips, Elbit Systems of America  
Jose Rios, Endicott Interconnect Technologies Inc  
Leo Lambert, EPTAC Corporation  
Terry Munson, Foresite, Inc.  
Martin Bayes, Four Square Consulting  
Graham Naisbitt, Gen3 Systems Limited  
Brian Wardhaugh, Gen3 Systems Limited  
Gregg Klawson, General Dynamics - C4 Systems  
Brian Toleno, Henkel Corporation  
Kristen Troxel, Hewlett-Packard Company  
Patrick O'Keefe, Holaday Circuits Inc.  
Richard Davidson, Honeywell Aerospace  
Raiyomand Aspandiar, Intel Corporation  
Jagadeesh Radhakrishnan, Intel Corporation  
Reza Ghaffarian, Jet Propulsion Laboratory  
Byron Case, L-3 Communications  
Bradley Toone, L-3 Communications  
William Fox, Lockheed Martin Missile & Fire Control  
Vijay Kumar, Lockheed Martin Missile & Fire Control

Linda Woody, Lockheed Martin Missile & Fire Control  
Beatriz Bennett, Lockheed Martin Missiles & Fire Control  
C. Don Dupriest, Lockheed Martin Missiles & Fire Control  
Steven Nolan, Lockheed Martin Mission Systems & Training  
John Potenza, Lockheed Martin Mission Systems & Training  
Hue Green, Lockheed Martin Space Systems Company  
Dennis Fritz, MacDermid, Inc.  
Lenora Toscano, MacDermid, Inc.  
Tom Fujikawa, Malcomtech International  
Russell Shepherd, Microtek Laboratories Anaheim  
James, Clark Multek Flexible Circuits, Inc.  
Christopher Hunt, National Physical Laboratory  
Darrell Freiwald, Northrop Grumman  
Mahendra Gandhi, Northrop Grumman Aerospace Systems  
William Miller, Panasonic Automotive Systems Company of America  
Mumtaz Bora, Peregrine Semiconductor  
Michah Pledger, Pledger Consulting  
Richard Kraszewski, Plexus Corp.  
Ursula Marquez de Tino, Plexus Corporation

---

Bill Bear, Raytheon Company	Srinivas Chada, Schlumberger Well Services	Calette Chamness, U.S. Army Aviation & Missile Command
Richard Iodice, Raytheon Company	Mary Petrusek, Schlumberger Well Services	Crystal Vanderpan, UL LLC
Roger Miedico, Raytheon Company	Henry Rekers, Schneider Electric	Ty Gragg, Unicircuit Inc.
Jeff Shubrooks, Raytheon Company	Gerard O'Brien, Solderability Testing & Solutions, Inc.	Donald Gudeczauskas, Uyemura International Corp.
Bill Vuono, Raytheon Company	Stephen Meeks, St. Jude Medical	George Milad, Uyemura International Corp.
Martin Scionti, Raytheon Missile Systems	David Sommervold, The Bergquist Company, Prescott	Wendi Boger, Viasystems Group, Inc.
Wesley Wolverton, Raytheon Systems Company	Elizabeth Allison, Trace Laboratories - Baltimore	Mike Hill, Viasystems Group, Inc.
Jason Koch, Robisan Laboratory Inc.	Renee Michalkiewicz, Trace Laboratories - Baltimore	Randy Reed, Viasystems Group, Inc.
Chris Mahanna, Robisan Laboratory Inc.	Debora Obitz, Trace Laboratories - Baltimore	Juan Vasquez, Viasystems Group, Inc.
David Adams, Rockwell Collins	James Monarchio, TTM Technologies, Inc.	Zhe (Jacky) Liu, ZTE Corporation
Robert Bagsby, Rockwell Collins		Jianfeng Liu, ZTE Corporation
Rachel Grinvalds, Rockwell Collins		Jiamin Zhang, ZTE Corporation
David Hillman, Rockwell Collins		Gerard Donovan
Gaston Hidalgo, Samsung Telecommunications America		John Rohlfing

---

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# Solderability Tests for Printed Boards

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## 1 GENERAL

**1.1 Scope** This standard prescribes test methods, defect definitions, and illustrations for assessing the solderability of printed wiring board surface conductors, attachment lands, and plated-through holes. This standard is intended for use by both vendor and user.

This standard is not intended to verify the potential of successful processing at assembly or to evaluate design impact on wettability. This specification describes procedures or methods to determine the acceptable wettability of a surface finish. Wettability can be affected by handling, finish application, and environmental conditions.

**1.2 Purpose** This standard describes solderability determinations that are made to verify that the printed board fabrication processes and subsequent storage have had no adverse effect on the solderability of those portions of the printed board intended to be soldered. Reference coupons or representative portions of a printed board may be used. Solderability is determined by evaluation of a test specimen which has been processed as part of a panel of boards and subsequently removed for testing per the method selected.

**1.3 Objective** To provide solderability test methods to determine the acceptance of printed board surface conductors, attachment lands, and plated-through holes to wet easily with solder, and to withstand the rigors of the printed board assembly processes.

**1.3.1 Definition of Requirements** The word “**shall**” is used in the text of this document wherever there is a requirement for materials, preparation, process control, or acceptance of a soldered connection or a test method. The word “**should**” reflects “best processing techniques” and is used to reflect general industry practices and a suggestion for guidance only.

**1.3.2 Document Hierarchy** In the event of conflict, the following descending order of precedence applies:

- a. Procurement documentation as agreed between user and supplier, which should include expected shelf life requirements if stored and handled properly.
- b. Master drawing or master assembly drawing reflecting the user’s detailed requirements.
- c. When required by the customer or per contractual agreement, this document, J-STD-003.
- d. Other documents, to the extent specified by the customer.

**1.4 Classification** Three general classes have been established to reflect progressive increases in sophistication, functional performance requirements, and testing/ inspection frequency as defined in the IPC-6010 series of documents.

The user is responsible for defining the product class. The product class should be stated in the procurement documentation package.

### **CLASS 1 General Electronic Products**

Includes products suitable for applications where the major requirement is function of the completed assembly.

### **CLASS 2 Dedicated Service Electronic Products**

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically the end-use environment would not cause failures.

### **CLASS 3 High Performance Electronic Products**

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

Circuit board performance classes do not dictate the surface finish durability rating that may be specified. Category 2/ Category A durability is the default coating durability rating.