JEDEC STANDARD

Serial Flash Discoverable Parameters (SFDP)

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SERIAL FLASH DISCOVERABLE PARAMETERS (SFDP) STANDARD

Contents

Foreword

This standard was prepared by the JEDEC SFDP Task Group authorized by the JC-42.4 Committee Chairman. It was derived from prior work done by Intel on their 'Serial Flash Discoverable Parameters Guidelines' document.

The intended audience is serial flash vendors and engineers writing device drivers for SFDP compliant serial flash devices.

The participating SFDP TG members were volunteers from AMD, ASPEED, Emulex, HP, Intel, Macronix, Micron, Microchip, Sanyo, Spansion, and Winbond.

Introduction

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors.

The SFDP standard defines a common parameter table describing important device characteristics and serial access methods used to read the parameter table data. Special Function parameter tables for erase sector address map and 4-byte address instructions are added in this revision of this standard. Additional parameter headers and tables can be specified by future revisions of this standard or by flash vendors and are optional.

SERIAL FLASH DISCOVERABLE PARAMETERS (SFDP) STANDARD

(From JEDEC Board Ballot JCB-14-08, formulated under the cognizance of the JC-42.4 Committee on Nonvolatile Memory.)

1 Scope

The SFDP standard defines the structure of the SFDP database within the memory device and methods used to read its data.

The JEDEC-defined header with Parameter ID FF00h and the related Basic Parameter Table is mandatory. This header and table provide basic information for a Serial Peripheral Interface (SPI) protocol memory. Additional headers and tables are optional.

The read command protocol using various I/O modes and standard clock rate are specified. The device electrical parameters are not specified.

2 Normative reference

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

1. JEP106, Standard Manufacturers Identification Code (contact jedec.org for the latest revision of this document)

2. NIST SP800-147, BIOS Protection Guidelines (http://csrc.nist.gov/publications/nistpubs/)

3 Terms and definitions

For the purposes of this standard, the following terms and definitions apply:

00b: The ‘b’ suffix indicates the ‘00’ digits are a binary representation of the number.

00h: The ‘h’ suffix indicates the ‘00’ digits are a hexadecimal representation of the number.

0x00: The ‘0x’ prefix indicates the ‘00’ digits are a hexadecimal representation of the number. This form is used in the ‘C’ sample code in Annexes.

Address: The three or four byte value following some instructions that is used to select a location within an address space of the flash memory.