

# JEDEC STANDARD

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## GRAPHICS DOUBLE DATA RATE (GDDR5) SGRAM STANDARD

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JESD212C

(Revision of JESD212B.01, December 2013)

FEBRUARY 2016

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Published by  
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Suite 240 South  
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## GRAPHICS DOUBLE DATA RATE (GDDR5) SGRAM STANDARD

(From JEDEC Board Ballot JCB-16-53, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories.)

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### **1 SCOPE**

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This document defines the Graphics Double Data Rate 5 (GDDR5) Synchronous Graphics Random Access Memory (SGRAM) standard, including features, functionality, package, and pin assignments. This scope may be expanded in future to also include other higher density devices.

The purpose of this Standard is to define the minimum set of requirements for JEDEC standard compatible 512 Mb through 8 Gb x32 GDDR5 SGRAM devices. System designs based on the required aspects of this standard will be supported by all GDDR5 SGRAM vendors providing JEDEC standard compatible devices. Some aspects of the GDDR5 standard such as AC timings and capacitance values were not standardized. Some features are optional and therefore may vary among vendors. In all cases, vendor data sheets should be consulted for specifics.

This standard was created based on the DDR Standard (JESD79) and some aspects of the GDDR4 Standard (JESD21C - 3.11.5.8). Each aspect of the changes for high speed operation were considered and balloted. The accumulation of these ballots were then incorporated to prepare this GDDR5 SGRAM document, replacing whole sections and incorporating the changes into Functional Description and Operation.