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IC Latch-Up Test

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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IC LATCH-UP TEST

(From JEDEC Board Ballots JCB-16-08, formulated under the cognizance of JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This standard covers the I-test and V_{supply} overvoltage latch-up testing of integrated circuits.

The purpose of this standard is to establish a method for determining IC latch-up characteristics and to define latch-up detection criteria. Latch-up characteristics are extremely important in determining product reliability and minimizing No Trouble Found (NTF) and Electrical Overstress (EOS) failures due to latch-up. This test method is applicable to NMOS, CMOS, bipolar, and all variations and combinations of these technologies.

NOTE As these technologies have evolved, it has been necessary to adjust this document to the realities of characterization with limits not imagined when the first latch-up document was generated some 25 years ago. Though it would be simpler to make the original limits of 1.5 times the maximum pin operating voltage an absolute level of goodness, the possibilities of success at this level are limited by the very low voltage technologies, and the medium and high voltage CMOS, BiCMOS and Bipolar technologies (>12 V). The concept of maximum stress voltage (MSV) allows the supplier to characterize latch-up in a way that differentiates between latch-up and EOS. This revision will make it more transparent to the end user that given the limits of certain technologies the subsequent latch-up characterizations are valid.

1.1 Classification

There are two classes for latch-up testing.

- Class I is for testing at room temperature ambient.
- Class II is for testing at the maximum operating ambient temperature (T_a) or maximum operating case temperature (T_c) or maximum operating junction temperature (T_j) in the data sheet.

For Class II testing at the maximum operating T_a or T_c, the ambient temperature or case temperature (T_c) shall be established at the required test value. For Class II testing at the maximum operating T_j, the ambient temperature T_a or the case temperature T_c should be selected to achieve a temperature characteristic of the junction temperature for a given device operating mode(s) during latch-up testing. The maximum operating ambient or case temperature during stress may be calculated based on the methods detailed in Annex B. The values used in Class II testing shall be recorded in the final report.

NOTE Elevated temperature will reduce latch-up resistance, and class II testing is recommended for devices that are required to operate at elevated temperature.