

# **IPC-6018C**

**2016 - July**

## **Qualification and Performance Specification for High Frequency (Microwave) Printed Boards**

Supersedes IPC-6018B

November 2011

*An international standard developed by IPC*

*Association Connecting Electronics Industries*



---

**The Principles of Standardization**

In May 1995 the IPC's Technical Activities Executive Committee (TAEC) adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

**Standards Should:**

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

**Standards Should Not:**

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

**Notice**

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

**IPC Position Statement on Specification Revision Change**

It is the position of IPC's Technical Activities Executive Committee that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC publication is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision. Adopted October 6, 1998

**Why is there a charge for this document?**

Your purchase of this document contributes to the ongoing development of new and updated industry standards and publications. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards and publications development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low to allow as many companies as possible to participate. Therefore, the standards and publications revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards and publications, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit [www.ipc.org](http://www.ipc.org) or call 847/597-2872.

Thank you for your continued support.



IPC-6018C

# **Qualification and Performance Specification for High Frequency (Microwave) Printed Boards**

Developed by the High Speed/High Frequency Board Performance Subcommittee (D-22) of the High Speed/High Frequency Committee (D-20) of IPC

***Supersedes:***

IPC-6018B – November 2011

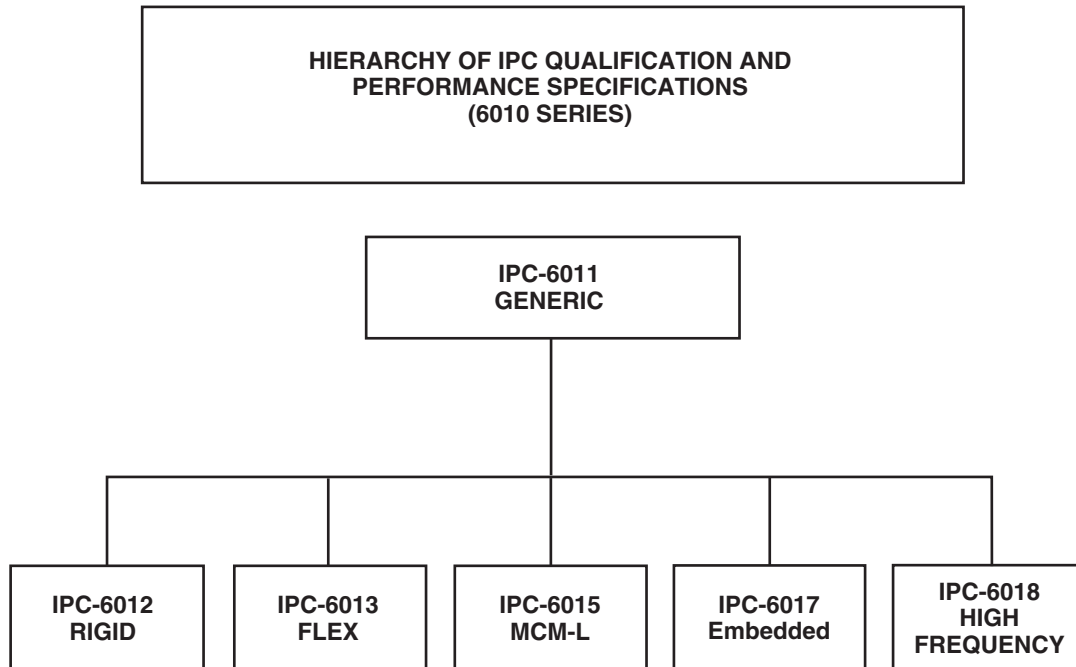
IPC-6018A – January 2002

IPC-6018 – January 1998

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC  
3000 Lakeside Drive, Suite 105N  
Bannockburn, Illinois  
60015-1249  
Tel 847 615.7100  
Fax 847 615.7105



## FOREWORD

This specification is intended to provide information on the detailed performance criteria of high frequency printed boards. It supersedes IPC-6018B and was developed as a revision to that document. The information contained herein is also intended to supplement the generic requirements identified in IPC-6011. When used together, these documents should lead both manufacturer and customer to consistent terms of acceptability.

IPC's documentation strategy is to provide distinct documents that focus on specific aspects of electronic packaging issues. In this regard, document sets are used to provide the total information related to a particular electronic packaging topic. A document set is identified by a four digit number that ends in zero (0) (i.e., IPC-6010).

Included in the set is the generic information, which is contained in the first document of the set. The generic specification is supplemented by one or multiple performance documents, each of which provide a specific focus on one aspect of the topic or the technology selected.

Failure to have all information available prior to building a board may result in a conflict in terms of acceptability.

As technology changes, a performance specification will be updated, or new focus specifications will be added to the document set. IPC invites input on the effectiveness of the documentation and encourages user response through completion of "Suggestions for Improvement" forms located at the end of each document.

## Acknowledgment

Any document involving a complex technology draws material from a vast number of sources across many continents. While the principal members of the High Speed/High Frequency Board Performance Subcommittee (D-22) of the High Speed/High Frequency Committee (D-20) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

<b>High Speed/High Frequency Committee</b>	<b>High Speed/High Frequency Board Performance Subcommittee</b>	<b>Technical Liaison of the IPC Board of Directors</b>
Chair Lance Auer Raytheon Missile Systems	Chair Lance Auer Raytheon Missile Systems	Bob Neves Microtek (Changzhou) Laboratories
Vice-Chair Don DeGroot Connected Community Networks, Inc.	Vice-Chair Mahendra Gandhi Northrop Grumman Aerospace Systems	
<b>High Speed/High Frequency Board Performance Subcommittee</b>		
Elizabeth A. Allison, NTS - Baltimore	Ayn Fuller, Northrop Grumman Corporation	Joseph Parrish, Northrop Grumman Corporation
John Andresakis, Park Electrochemical Corp.	Ty Gragg, Unicircuit Inc. Louis J. Hart, Compunetics Inc.	Gerry Partida, Marcel Electronics International
Filbert Arzola, Raytheon Company	Philip M. Henault, Raytheon Company	Stephen Pierce, SGP Ventures, Inc.
Jimmy Baccam, Lockheed Martin Missiles & Fire Control	Dana W. Korf, Multek Electronics Limited	Melvin L. Pollard, Northrop Grumman Corporation
Robert J. Black, Northrop Grumman Corporation	Kelly Kovalovsky, i3 Electronics	Randy R. Reed, R. Reed Consultancy LLC
Scott A. Bowles, L-3 Fuzing and Ordnance Systems, Cincinnati	William Kummer, Raytheon Company	Jose A. Rios, Massachusetts Institute of Technology
Steven A. Bowles, L-3 Fuzing and Ordnance Systems, Cincinnati	Mark Lecuyer, Raytheon Systems Company	Edward Sandor, Taconic Advanced Dielectric Division
Mark Buechner, BAE Systems	John Leschisin, Minco Products, Inc.	Karl A. Sauter, Oracle America, Inc.
Brian D. Butler, Introbotix Corporation	Jeff Lewis, Holaday Circuits Inc. Clifford R. Maddox, Boeing Company	Tony R. Senese, Panasonic Industrial Devices Sales Company of America (PIDSA)
Byron Case, L-3 Communications	Chris Mahanna, Robisan Laboratory Inc.	Gilbert Shelby, Raytheon Systems Company
Denise Chevalier, Amphenol Printed Circuits, Inc.	Rene Martinez, Northrop Grumman Aerospace Systems	Russell S. Shepherd, National Technical Systems Anaheim
Kelly M. Daniluk, NASA Goddard Space Flight Center	Thomas McCarthy, Taconic Advanced Dielectric Division	Andy Slade, Rogers Corporation
Joseph Davis, Rogers Corporation	James J. Monarchio, TTM Technologies, Inc.	Bhanu Sood, NASA Goddard Space Flight Center
Don DeGroot, Connected Community Networks, Inc.	Randal W. Oberle, Raytheon Systems Company	Brian Stevens, Rockwell Collins
Don Dupriest, Lockheed Martin Missiles & Fire Control	Christopher G. Olson, Rockwell Collins	Chris Totten, Isola Group SARL
Patricia S. Dupuis, Raytheon Company	William A. Ortloff, Raytheon Company	Crystal E. Vanderpan, UL LLC
Robert Farfan, TTM Technologies		Jennet Volden, Rockwell Collins
Gary M. Ferrari, FTG Circuits		Dan Welch, Rogers Corporation
Sandra M. Fortune, Northrop Grumman Corporation		

This Page Intentionally Left Blank

# Table of Contents

<b>1</b>	<b>SCOPE</b>	1	3.2.9	Fusing Fluids and Fluxes	12
1.1	Statement of Scope	1	3.2.10	Marking Inks	12
1.2	Purpose	1	3.2.11	Hole Fill Insulation Material	12
1.3	Performance Classification and Types	1	3.2.12	Metal and/or Composite, External	12
1.3.1	Classifications	1	3.2.13	Via Protection	12
1.3.2	Printed Board Type	1	3.2.14	Embedded Passive Materials	12
1.3.3	Selection for Procurement	1	3.3	Visual	12
1.3.4	Material, Plating Process and Final Finish	3	3.3.1	Edges of Microwave Printed Boards	12
1.4	Terms and Definitions	3	3.3.2	Laminate Imperfections	12
1.4.1	White Spots	3	3.3.3	Plating and Coating Voids in the Hole	13
1.4.2	Hybrid (Composite) Printed Board	3	3.3.4	Lifted Lands	14
1.4.3	As Agreed Between User and Supplier (AABUS)	3	3.3.5	Marking	14
1.4.4	High Density Interconnects (HDI)	4	3.3.6	Solderability	14
1.5	Interpretation	4	3.3.7	Plating Adhesion	14
1.6	Presentation	4	3.3.8	Edge Printed Board Contact, Junction of Gold Plate to Solder Finish	15
1.7	Revision Level Changes	4	3.3.9	Workmanship	15
1.8	Master Drawing	4	3.4	Printed Board Dimensional Requirements	15
<b>2</b>	<b>APPLICABLE DOCUMENTS</b>	4	3.4.1	Hole Size, Hole Pattern Accuracy, Pattern Feature Accuracy and Slots	15
2.1	IPC	4	3.4.2	Annular Ring and Breakout (External)	16
2.2	Joint Industry Standards	6	3.4.3	Bow and Twist	17
2.3	Federal	6	3.5	Conductor Definition	18
2.4	American Society for Testing and Materials	6	3.5.1	Undercutting	18
2.5	Underwriters Lab	6	3.5.2	Conductor Widths and Thicknesses and Spacing	18
2.6	National Electrical Manufacturers Association	7	3.5.3	Conductive Surfaces	19
2.7	American Society for Quality	7	3.6	Structural Integrity	21
2.8	AMS	7	3.6.1	Thermal Stress Testing	22
2.9	American Society of Mechanical Engineers	7	3.6.2	Requirements for Microsectioned Coupons or Printed Boards	23
<b>3</b>	<b>REQUIREMENTS</b>	7	3.7	Solder Mask Requirements on non-PTFE laminates	36
3.1	General	7	3.7.1	Solder Mask Coverage	36
3.2	Materials Used in this Specification	7	3.7.2	Solder Mask Cure and Adhesion	37
3.2.1	Laminates and Bonding Material for Multilayer or Mixed Dielectric Printed Boards	7	3.7.3	Solder Mask Thickness	37
3.2.2	External Bonding Materials	7	3.8	Electrical Requirements	37
3.2.3	Other Dielectric Materials	7	3.8.1	Dielectric Withstanding Voltage	37
3.2.4	Metal Foils	7	3.8.2	Electrical Continuity and Isolation Resistance	38
3.2.5	Metal Core/Backed	8	3.8.3	Circuit Shorts	38
3.2.6	Base Metallic Plating Depositions and Conductive Coatings	8	3.8.4	Circuit/PTH Shorts to Metal Substrate	38
3.2.7	Final Finish Depositions and Coatings – Metallic and Nonmetallic	8	3.8.5	Moisture and Insulation Resistance (MIR)	38
3.2.8	Polymer Coating (Solder Mask)	12	3.8.6	Dielectric Withstanding Voltage After MIR	38

3.9	Cleanliness .....	38	Figure 3-4	Breakout of 90° and 180° .....	17
3.9.1	Cleanliness Prior to Solder Mask Application .....	38	Figure 3-5	Usage of Modified Land Shapes in Breakout Conditions .....	17
3.9.2	Cleanliness After Solder Mask, Solder, or Alternative Surface Coating Application .....	38	Figure 3-6	Example of Intermediate Target Land in a Microvia .....	17
3.9.3	Cleanliness of Inner Layers After Oxide Treatment Prior to Lamination .....	38	Figure 3-7	Conductor Edge Definitions .....	18
3.10	Special Requirements .....	38	Figure 3-8	Undercut .....	18
3.10.1	Outgassing .....	39	Figure 3-9	Rectangular Surface Mount Lands .....	20
3.10.2	Fungus Resistance .....	39	Figure 3-10	Round Surface Mount Lands .....	20
3.10.3	Vibration .....	39	Figure 3-11	Printed Board Edge Connector Lands .....	21
3.10.4	Mechanical Shock .....	39	Figure 3-12	Plated Hole Microsection (Grinding/Polishing) Tolerance .....	22
3.10.5	Impedance Testing .....	39	Figure 3-13	An Example of Plating to Target Land Separation .....	23
3.10.6	Coefficient of Thermal Expansion (CTE) .....	39	Figure 3-14	Separations at External Foil .....	25
3.10.7	Thermal Shock .....	39	Figure 3-15	Crack Definition .....	25
3.10.8	Surface Insulation Resistance (As Received) .....	39	Figure 3-16	Plating Folds/Inclusions – Minimum Measurement Points .....	25
3.10.9	Wire Bond Adhesion .....	39	Figure 3-17	Typical Microsection Evaluation Specimen .....	26
3.10.10	Die Bond Adhesion .....	39	Figure 3-18	Measurement for Dielectric Removal .....	26
3.10.11	Rework Simulation .....	40	Figure 3-19	Etchback in Contact with PTFE Layer .....	27
3.10.12	Metal Core (Horizontal Microsection) .....	40	Figure 3-20	Measurement Locations for PTFE Resin Smear .....	27
3.10.13	Peel Strength Requirements (For Foil Laminated Construction Only) .....	40	Figure 3-21	Negative Etchback .....	28
3.10.14	Destructive Physical Analysis .....	40	Figure 3-22	Annular Ring Measurement (Internal) .....	28
3.10.15	Lap Shear .....	40	Figure 3-23	Microsection Rotations for Breakout Detection .....	29
3.11	Repair .....	40	Figure 3-24	Comparison of Microsection Rotations .....	29
3.11.1	Circuit Repairs .....	40	Figure 3-25	Example of Nonconforming Dielectric Spacing Reduction Due to Breakout at Microvia Target Land .....	30
3.12	Rework .....	40	Figure 3-26	Surface Copper Wrap Measurement for Filled Holes .....	30
<b>4</b>	<b>QUALITY ASSURANCE PROVISIONS</b> .....	<b>40</b>	Figure 3-27	Surface Copper Wrap Measurement for Nonfilled Holes .....	30
4.1	General .....	40	Figure 3-28	Wrap Copper in Type 4 Printed Board (Acceptable) .....	31
4.1.1	Qualification .....	41	Figure 3-29	Wrap Copper Removed by Excessive Sanding/Planarization/Etching (Not Acceptable) .....	31
4.1.2	Sample Test Coupons .....	41	Figure 3-30	Copper Cap Thickness .....	32
4.2	Acceptance Tests .....	42	Figure 3-31	Copper Cap Filled Via Height (Bump) .....	32
4.2.1	C=0 Zero Acceptance Number Sampling Plan .....	42	Figure 3-32	Copper Cap Depression (Dimple) .....	32
4.2.2	Referee Tests .....	42	Figure 3-33	Copper Cap Plating Voids .....	32
4.3	Quality Conformance Testing .....	42	Figure 3-34	Example of Acceptable Voiding in a Cap Plated, Copper Filled Microvia .....	33
4.3.1	Coupon Selection .....	42	Figure 3-35	Example of Acceptable Voiding in a Copper Filled Microvia without Cap Plating .....	33
<b>5</b>	<b>PACKAGING</b> .....	<b>47</b>	Figure 3-36	Example of Nonconforming Void in a Cap Plated, Copper Filled Microvia .....	33
<b>6</b>	<b>NOTES</b> .....	<b>47</b>	Figure 3-37	Example of Nonconforming Void in a Copper Filled Microvia .....	33
6.1	Ordering Data .....	47	Figure 3-38	Microvia Contact Dimension .....	33
6.2	Superseded Specifications .....	47			
<b>Figures</b>					
Figure 3-1	Microvia Definition .....	8			
Figure 3-2	Adhesive Band Near Exposed Conductor .....	15			
Figure 3-3	Annular Ring Measurement (External) .....	17			

Figure 3-39 Exclusion of Separations in Microvia Target Land Contact Dimension ..... 33

Figure 3-40 Penetration of Microvia Target Land ..... 34

Figure 3-41 Metal Core to PTH Spacing ..... 35

Figure 3-42 Measurement of Minimum Dielectric Spacing ..... 35

Figure 3-43 Fill Material in Blind/Through Vias When Cap Plating Not Specified ..... 36

Table 3-8 Edge Board Contact Gap ..... 15

Table 3-9 Minimum Annular Ring ..... 16

Table 3-10 Maximum Percent of Allowable Conductor Width Deviations ..... 18

Table 3-11 Percent of Allowable Conductor Space Deviations ..... 19

Table 3-12 Percent of Allowable Conductor Width Reduction Caused By Pin Holes ..... 19

**Tables**

Table 1-1 Default Requirements ..... 2

Table 1-2 Technology Adder Examples ..... 2

Table 3-1 Metal Core Substrate ..... 8

Table 3-2 Maximum Limits of SnPb Solder Bath Contaminant ..... 9

Table 3-3 Final Finish and Coating Requirements ..... 10

Table 3-4 Surface and Hole Copper Plating Minimum Requirements for Buried Vias > 2 Layers, Through-Holes, and Blind Vias ..... 11

Table 3-5 Surface and Hole Copper Plating Minimum Requirements for Microvias (Blind and Buried) ..... 11

Table 3-6 Surface and Hole Copper Plating Minimum Requirements for Buried via cores (2 layers) ..... 11

Table 3-7 Plating and Coating Voids Visual Examination ..... 13

Table 3-13 Percent of Reduction In Dielectric Material Thickness ..... 19

Table 3-14 Plated-Through Hole Integrity After Stress ..... 24

Table 3-15 Cap Plating Requirements for Filled Holes ..... 32

Table 3-16 Microvia Contact Dimension ..... 34

Table 3-17 Internal Layer Foil Thickness after Processing ..... 34

Table 3-18 External Conductor Thickness after Plating ..... 35

Table 3-19 Solder Mask Adhesion ..... 37

Table 3-20 Dielectric Withstanding Voltages ..... 37

Table 3-21 Insulation Resistance ..... 38

Table 4-1 Qualification Test Coupons ..... 41

Table 4-2 C=0 Sampling Plan per Lot Size ..... 42

Table 4-3 Acceptance Testing and Frequency ..... 43

Table 4-4 Quality Conformance Testing ..... 47

This Page Intentionally Left Blank

# Qualification and Performance Specification for High Frequency (Microwave) Printed Boards

## 1 SCOPE

**1.1 Statement of Scope** This specification covers end product inspection and test of high frequency (microwave) printed boards for microstrip, stripline, mixed dielectric and multilayer stripline applications with or without buried/blind vias, and metal cores. The printed board may contain embedded active or passive circuitry with distributive capacitive planes, capacitive or resistive components conforming to IPC-6017. The printed board may contain build up High Density Interconnect (HDI) layers.

**1.2 Purpose** The purpose of this specification is to provide requirements for qualification and performance of high frequency (microwave) printed boards.

### 1.3 Performance Classification and Types

**1.3.1 Classifications** This specification establishes acceptance criteria for the performance classification of high frequency printed boards based on customer and/or end-use requirements. Printed boards are classified by one of three general Performance Classes as defined in IPC-6011.

**1.3.1.1 Requirement Deviations** Requirements deviating from these heritage classifications **shall** be as agreed between user and supplier (AABUS).

**1.3.1.2 Space and Military Avionics Requirement Deviations** Space and military avionics performance classification deviations are provided in the IPC-6018CS Addendum and are applicable when the addendum is specified within the procurement documentation.

**1.3.2 Printed Board Type** This specification will define eight types of high frequency (microwave) printed boards.

*Type 1* – Single Sided

*Type 2* – Double Sided

*Type 3* – Homogeneous Dielectric Multilayer Construction

*Type 4* – Mixed Dielectric Multilayer

*Type 5* – Homogeneous Dielectric Multilayer with blind and/or buried vias

*Type 6* – Mixed Dielectric Multilayer with blind and/or buried vias

*Type 7* – Metal and/or composite backed printed boards, single sided or double sided

*Type 8* – Multilayer metal and/or composite backed or core printed boards with or without blind and/or buried vias

**1.3.3 Selection for Procurement** For procurement purposes, Performance Class **shall** be specified in the procurement documentation.

The documentation **shall** provide sufficient information to the supplier so that he can fabricate the printed board and ensure that the user receives the desired product. Information that should be included in the procurement documentation is to be in accordance with IPC-2611 and IPC-2614.

The procurement documentation should specify the thermal stress test method to be used to meet the requirement of 3.6.1. Selection **shall** be from those depicted in 3.6.1.1, 3.6.1.1.1, 3.6.1.2 and 3.6.1.3. If not specified (see 6.1), the default **shall** be per Table 1-1.

During the selection process, the user should take into consideration the following when determining the appropriate thermal stress test method:

- Wave solder, selective solder, hand solder assembly processes (see 3.6.1.1 and 3.6.1.1.1)
- Conventional (eutectic) reflow processes (see 3.6.1.2)
- Lead-free reflow processes (see 3.6.1.3)

IPC-6016, a sectional performance specification for HDI printed boards, was cancelled by the IPC. Relevant HDI conformance and acceptance criteria has been transferred to this revision of this specification.