

JEDEC STANDARD

Byte Addressable Energy Backed Interface

JESD245A

(Revision of JESD245, December 2015)

SEPTEMBER 2016

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2016
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

BYTE ADDRESSABLE ENERGY BACKED INTERFACE, VERSION 2.0 DRAFT 3**Contents**

	Page
Foreword	ii
Introduction	ii
1 Scope	1
2 Normative references	1
3 Terms and definitions	1
4 Introduction	5
5 I ² C	6
6 Serial Presence Detect	12
7 Features	13
8 Register Map	23
9 Host Operation Workflows	95
Annex A	
Annex B Differences between revisions	
Figures	
1 NVDIMM overview	6
2 Legend for I ² C operations	7
3 I ² C Read Byte	8
4 I ² C Write Byte	8
5 I ² C Block Read	8
6 I ² C Block Write	9
7 I ² C paging mechanism	11
8 SAVE_N trigger mode timing diagram	70
Tables	
1 Required SPD fields	13
2 Firmware image header	21
3 Temperature value bit definition	23
4 Page 0 categories	24
5 Page 0 register map	25
6 Timing	69
7 Page 1 categories	71
8 Page 1 register map	71
9 Page 2 categories	79
10 Page 2 register map	79
11 Page 3 categories	89
12 Page 3 register map	89

Foreword

This standard has been prepared by JEDEC. The purpose of this standard is definition of an energy backed byte addressable function on a non-volatile dual in-line memory module (NVDIMM). This standard defines the feature set and commands implemented by the energy backed byte addressable function on the NVDIMM.

Introduction

NVDIMM is a DDR-based memory module that can be integrated into a standard platform. An Energy Backed Byte Addressable Function on a NVDIMM is designed to preserve data in the event of the power failure. An Energy Backed Byte Address Function is backed by a combination of SDRAM and non-volatile memory (e.g., NAND flash) on the NVDIMM. It operates at DDR speeds and can provide persistent storage by backing up the SDRAM contents into the non-volatile memory in the event of a power failure. This is made possible by an Energy Source (e.g., super-capacitor) which maintains charge on the module enabling back-up of data from SDRAM to the non-volatile memory, providing a storage-class memory solution.

To be able to provide interoperability and the ability for platform and platform software (e.g., BIOS) to support NVDIMMs from various manufacturers, standardization of the host to module interface, discovery mechanism, the feature set and command operations are required, as described in this document.

BYTE ADDRESSABLE ENERGY BACKED INTERFACE

(From JEDEC Board Ballot JCB-16-25, formulated under the cognizance of the JC-45.6 Subcommittee on Hybrid Modules. Item 2233.22)

1 Scope

This standard specifies the host and device interface for a DDR4 DIMM interface module that achieves non-volatility by copying SDRAM contents into non-volatile memory when Host power is lost using an Energy Source managed by either the module or the Host.

Although this standard is targeted towards DDR4 NVDIMM only, it does not preclude adoption of this standard by other implementations (e.g., DDR3 NVDIMM).

2 Normative References

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated. For undated references, the latest edition of the normative document referred to applies.

DDR4 SPD Contents NVDIMM Revision 0.5

JESD21C, SPD4_01_06, *EE1004 and TSE2004 Device Specification*

I²C Bus Specification Revision 4

System Management Bus (SMBus) Specification Version 2.0

DDR4 RCD02 Specification

DDR4 DB02 Specification