

JEDEC PUBLICATION

Failure Mechanisms and Models for Semiconductor Devices

JEP122H

(Revision of JEP122G, October 2011)

SEPTEMBER 2016

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2016
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

FAILURE MECHANISMS AND MODELS FOR SEMICONDUCTOR DEVICES

Contents

| | Page |
|---------------------------------------------------------------------------|------|
| Foreword | iii |
| Introduction | iii |
| 1 Scope | 1 |
| 2 Terms and definitions | 1 |
| 3 Inclusions, deliberate omissions, and resources | 5 |
| 4 The basic thermal acceleration equation | 9 |
| 5 Models for common failure mechanisms | 9 |
| FEOl Failure Mechanisms | |
| 5.1 Time-Dependent Dielectric Breakdown (TDDB) – gate oxide | 9 |
| 5.2 Hot Carrier Injection (HCI) | 14 |
| 5.3 Negative Bias Temperature Instability (NBTI) | 17 |
| 5.4 Surface inversion (mobile ions) | 19 |
| 5.5 Floating-Gate Nonvolatile Memory Data Retention | 21 |
| 5.6 Localized Charge Trapping Nonvolatile Memory Data Retention | 29 |
| 5.7 Phase Change (PCM) Nonvolatile Memory Data Retention | 31 |
| BEoL Failure Mechanisms | |
| 5.8 Time-Dependent Dielectric Breakdown (TDDB) – ILD/Low-k/Mobile Cu ion | 34 |
| 5.9 Aluminum Electromigration (Al EM) | 43 |
| 5.10 Copper Electromigration (Cu EM) | 46 |
| 5.11 Aluminum and Copper Corrosion | 48 |
| 5.12 Aluminum Stress Migration (Al SM) | 53 |
| 5.13 Copper Stress Migration (Cu SM) | 55 |
| Packaging/Interfacial Failure Mechanisms | |
| 5.14 Fatigue failure due to temperature cycling and thermal shock | 58 |
| 5.15 Interfacial failure due to temperature cycling and thermal shock | 63 |
| 5.16 Intermetallic and oxidation failure due to high temperature | 66 |
| 5.17 Tin Whiskers | 68 |
| 5.18 Ionic Mobility Kinetics (PCB) – Component Cleanliness | 72 |
| Statistics and Modeling Parameter Determination | |
| 5.19 Reliability data/analysis | 75 |
| 5.20 Design of Experiments (DOE) for determination of modeling parameters | 80 |
| 6 Activation energies and modeling factors | 82 |
| Annexes | |
| Annex A – List of references | 87 |
| Annex B – Differences between JEP122H and JEP122G | 103 |

FAILURE MECHANISMS AND MODELS FOR SEMICONDUCTOR DEVICES

Contents

| Figures | Page |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| 5.1-1 Photograph of TDDB breakdown in a gate oxide – mid-gate | 13 |
| 5.5-1 (a) Example of failure mechanisms scenario affecting ΔV_T during data retention (from [5.5.16]), and (b) extraction of E_{aa} for each mechanism (from [5.5.15]). | 22 |
| 5.5-2 (a) Spectrum of detrapping time constants immediately after cycling (black curve) and during data retention (red curves), and (b) Resulting $\langle \Delta V_T(t_R) \rangle$ transient. | 25 |
| 5.5-3 (a) Comparison of time constant spectra between uniform cycling of duration t_{cyc} and an equivalent cycling where all the delays are lumped in a single wait of duration $A \cdot t_{cyc}$ prior to the bake phase, and (b) Resulting $\langle \Delta V_T(t_R) \rangle$ transients. $A = 0.2$ results in similar V_T loss during data retention | 27 |
| 5.5-4 Extrapolation of SILC bit error rate | 28 |
| 5.8-1 Time-Dependent Dielectric Breakdown (TDDB) in various dielectrics | 35 |
| 5.8-2 Metal stack cross section/schematic | 37 |
| 5.8-3 Normal distribution of breakdown voltage | 38 |
| 5.8-4 Copper short/extrusion | 39 |
| 5.9-1 Examples of Aluminum Electromigration | 45 |
| 5.10-1 Examples of Copper Electromigration | 48 |
| 5.11-1 Aluminum bond pad corrosion | 52 |
| 5.11-2 Electrochemical reaction | 52 |
| 5.11-3 Corrosion rate versus surface mobility | 52 |
| 5.12-1 Examples of Aluminum Stress Migration | 55 |
| 5.13-1 Examples of Copper Stress Migration | 57 |
| 5.14-1 Examples of temperature cycling/thermal shock damage | 62 |
| 5.15-1 Example of interfacial delamination after temperature cycling | 65 |
| 5.17-1 SEM of Tin Whiskers on Matte Tin plated Alloy 42 leads [5.16.4] | 71 |
| 5.17-2 Optical Image of a Tin Whisker growing from Relay lead to case [5.16.3] | 71 |
| 5.17-3 FIB - matte tin whisker structure from a temperature cycled specimen [5.16.5] | 71 |
| 5.17-4 Optical Image - Tin Whisker growing from SAC 305 solder over Alloy 42 - matte tin | 71 |
| 5.17-5 Optical image of Tin Whisker on a copper coupon with matte tin plating [5.16.4] | 71 |
| 5.17-6 8 mm long Tin Whisker growing from a bracket holding electronics in a frame. | 71 |
| 5.17-7 Tin Whisker breaking through 10 μm Uralane 5750 coating (9 yr office storage) [5.16.3] | 71 |
| 5.18-1 Resistor corroded open due to trapped MSA residues in epoxy surface [3] | 73 |
| 5.18-2 Electrochemical migration between leads on a QFP | 73 |
| 5.18-3 Leakage and corrosion problems with residues on tinned leads due to aggressive flux | 74 |
| 5.18-4 Leakage & corrosion problems w/ BGA components between balls due to poorly cleaned water soluble solderpaste from ball attachment. | 74 |
| 5.18-5 Leakage due to large MSA levels on Chip capacitor. Sulfate levels of 24 $\mu\text{g}/\text{in}^2$ ($\sim 4 \mu\text{g}/\text{cm}^2$) | 74 |
| 5.19-1 Lognormal Distribution | 76 |
| 5.19-2 Weibull Distribution | 76 |
| 5.19-3 Tracking of lognormal and Weibull distributions | 77 |
| 5.19-4 Lognormal plotted as Weibull | 78 |
| 5.19-5 Weibull plotted as lognormal | 78 |
| | |
| Tables | |
| 5.14-1 Values for q for common ULSI material classes | 59 |
| 5.15-1 Values for the Paris Law exponent, m for several different interfacial fracture mechanisms | 64 |
| 5.17-1 Values for the Time-To-Whisker-Nucleation model for various conditions | 70 |
| 5.20-1 Example for temperature cycle schedule | 81 |
| 6-1 Failure Mechanisms and Model Parameters | 83 |

FAILURE MECHANISMS AND MODELS FOR SEMICONDUCTOR DEVICES

Foreword

This publication provides guidance in the selection of reliability modeling parameters, namely functional form, apparent thermal activation energy values, and sensitivity to stresses such as power supply voltage, substrate current, current density, gate voltage, relative humidity, temperature cycling range, mobile ion concentration, etc.

The failure mechanisms described in the several sections of this publication constitute commonly accepted industrial models, validated by a team of reliability experts (SEMATECH/ISMI Reliability Council) and buttressed by citations to the most cogent published literature.

Revisions have been made to reflect technology changes, especially as Cu now supplements Al and low-dielectric-constant insulators are complementing traditional silica.

Introduction

Accelerated tests are typically used to find and identify potential failure mechanisms in semiconductor devices and to estimate the rate of their occurrence in electronic systems. The historical approach to investigating the relationship between a maximum stress failure rate and a system failure rate is to choose a single representative "equivalent" apparent thermal activation energy for a given product or product group. A single, best-estimate apparent activation energy value facilitates accurate estimation of the acceleration factor for the device failure rate estimation in the system application.

A word about formats within this document: parentheses () enclose equation numbers; square brackets [] enclose citation numbers. All equation, citation, and figure numbers include the subclause number so that individual clauses can be modified without disturbing other clauses, except for page numbers. Thus, **(5.3.2)** is the 2nd equation in 5.3 and **[5.11.5]** is the 5th citation in 5.11. The citations can be found in Annex A.

FAILURE MECHANISMS AND MODELS FOR SEMICONDUCTOR DEVICES

(From JEDEC Board Ballot JCB-01-97, JCB-03-39, JCB-08-61, JCB-09-19, JCB-10-64, JCB-11-74, and JCB-16-32, formulated under the cognizance of JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This publication provides a list of failure mechanisms and their associated activation energies or acceleration factors that may be used in making system failure rate estimations when the only available data is based on tests performed at accelerated stress test conditions. The method to be used is the Sum-of-the-Failure-Rates method.

The models apply primarily to the following:

- a) Aluminum (doped with small amounts of Cu and/or Si) and copper alloy metallization
- b) Refractory metal barrier metals with thin anti-reflection coatings
- c) Doped silica or silicon nitride interlayer dielectrics, including low-dielectric-constant materials
- d) Poly silicon or "salicide" gates (metal-rich silicides such as W, Ni & Co to decrease resistivity)
- e) Thin SiO₂ gate dielectric
- f) Silicon with p-n junction isolation
- g) Tin Whisker Growth Kinetics
- h) Printed Circuit Board Ionic Mobility

2 Terms and definitions

For the purpose of this publication, the following terms and definitions apply.

acceleration factor (A, AF): For a given failure mechanism, the ratio of the time it takes for a certain fraction of the population to fail, following application of one stress or use condition, to the corresponding time at a more severe stress or use condition.

NOTE 1 Times are generally derived from modeled time-to-failure distributions (lognormal, Weibull, exponential, etc.).

NOTE 2 Acceleration factors can be calculated for temperature, electrical, mechanical, environmental, or other stresses that can affect the reliability of a device.

NOTE 3 Acceleration factors are a function of one or more of the basic stresses that can cause one or more failure mechanisms. For example, a plot of the natural log of the time-to-failure for a cumulative constant percentage failed (e.g., 50%) at multiple stress temperatures as a function of $1/kT$, the reciprocal of the product of Boltzmann's constant in electronvolts per kelvin and the absolute temperature in kelvins, is linear if one and only one failure mechanism is involved. The best-fit linear slope is equal to the apparent activation energy in electronvolts.

NOTE 4 The abbreviation AF is often used in place of the symbol A.

acceleration factor, stress (A_i): The acceleration factor due to the presence of some stress (e.g., current density, electric field, humidity, temperature cycling).