JEDEC STANDARD

Test Methods to Characterize Voiding in Pre-SMT Ball Grid Array Packages

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Introduction

As ball grid array component pitch continues to decrease, the need to characterize solder voiding has become more significant. Solder void manifestation (type and/or sizes) has been used to determine process capability as a means of quality assurance during process transfer, and as indicators of process stability from in-line manufacturing monitors. This document describes how to characterize voids in solder spheres in ball grid array packages prior to surface-mount (SMT) reflow soldering.

TEST METHODS TO CHARACTERIZE VOIDING IN PRE-SMT BALL GRID ARRAY PACKAGES

(From Board Ballot JCB-10-56, and JCB-16-18 formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

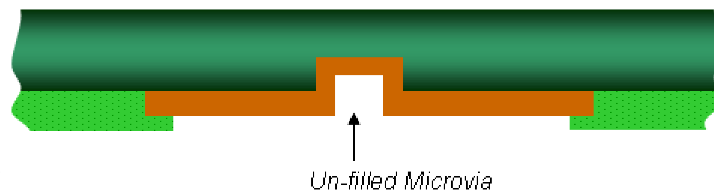
1 Scope

This publication provides an overview of solder void types, outlines current metrologies and test methods used for pre-SMPT solder void characterization and potential limitations, and prescribes sampling strategy for data collection, and tolerance guidelines for corrective measures.

Test methods can be applied to several types of ball grid array packages such as FCBGA, PBGA, CBGA, and CCGA with minimum 0.5 mm ball-to-ball pitch and constructed with leaded and lead-free solder alloys.

Guidelines for pre-SMT voids may not be sufficiently robust where ball grid array packages balls are assembled onto unfilled micro-via structures on package substrate land. Hence, the un-filled microvia construction (Figure 1-1a) is considered out-of-scope for this document, while filled via (Figure 1-1b) is within scope.

a) BGA Package Substrate with un-filled Microvia



b) BGA Package Substrate with filled Microvia

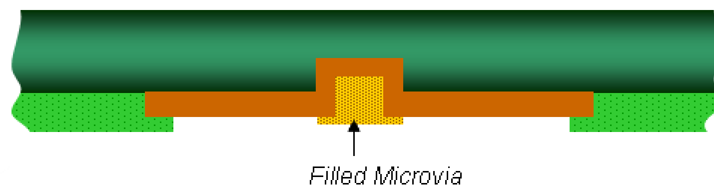


Figure 1-1 — Illustration of Un-filled Microvia (1-1a) out-of-scope vs. Filled Microvia (1-1b) in-scope of document