JEDEC STANDARD

Temperature, Bias, and Operating Life

JESD22- A108E

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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TEST METHOD A108E
TEMPERATURE, BIAS, AND OPERATING LIFE

(From JEDEC Board Ballots JCB-99-89, JCB-99-89A, JCB-05-49, JCB-10-60, and JCB-16-47 formulated under the cognizance of JC-14.1 Committee on Reliability Test Methods for Packaged Devices.)

1 Scope

This test is used to determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way, and is primarily for device qualification and reliability monitoring. A form of high temperature bias life using a short duration, popularly known as burn-in, may be used to screen for infant mortality-related failures. The detailed use and application of burn-in is outside the scope of this document.

1.1 Applicable documents

JESD47, *Stress-Test Driven Qualification of Integrated Circuits*

JEP122, *Failure Mechanism and Models for Silicon Semiconductor Devices*

2 Apparatus

The performance of this test requires equipment that is capable of providing the particular stress conditions to which the test samples will be subjected.

2.1 Circuitry

The circuitry through which the samples will be biased must be designed with several considerations:

2.1.1 Device schematic

The biasing and operating schemes must consider the limitations of the device and shall not overstress the devices or contribute to thermal runaway.

2.1.2 Power

The test circuit should be designed to limit power dissipation such that, if a device failure occurs, excessive power will not be applied to other devices in the sample.

2.2 Device mounting

Equipment design, if required, shall provide for mounting of devices to minimize adverse effects while parts are under stress, (e.g., improper heat dissipation).