JEDEC STANDARD

0.6 V Low Voltage Swing Terminated Logic (LVSTL06)

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0.6 V LOW VOLTAGE SWING TERMINATED LOGIC (LVSTL06)

(From JEDEC Board Ballot JCB-16-37, formulated under the cognizance of the JC-16 Committee on Interface Technology.

1 Scope

This standard defines power supply voltage range, dc interface, switching parameter and overshoot/undershoot for high speed low voltage swing terminated NMOS driver family digital circuits with 0.6V supply. The specifications in this standard represent a minimum set of interface specifications for low voltage terminated circuits.

The purpose of this standard is to provide a standard of specification for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users. Class 1 describes low VOH (Nominal VOH = VDDQ*0.5) level terminated electrical characteristics. Class 2 describes high VOH (Nominal VOH = VDDQ*0.6) level terminated electrical characteristics.

2 LVSTL system definition

LVSTL (Low Voltage Swing Terminated Logic) Driver and ODT System LVSTL I/O cell is comprised of pull-up, pull-down driver and a terminator. The basic cell is shown in **Figure** 1.

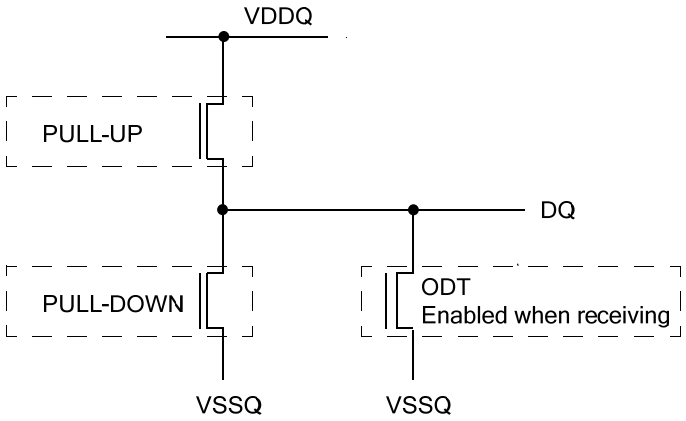

Figure 1 — LVSTL I/O Cell