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DDR4 Registering Clock Driver - DDR4RCD01

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1 Scope

This document defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the DDR4 Registering Clock Driver (RCD) with parity for driving address and control nets on DDR4 RDIMM and LRDIMM applications. Any TBDs as of this document, are under discussion by the formulating committee.

The terms ‘Registering Clock Driver’, ‘RCD’, ‘register’ or ‘device’ are used interchangeably to refer to this device in the remainder of this specification.

The purpose is to provide a standard for the DDR4RCD01 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation DDR4RCD01 refers to the part designation of a series of commercial logic parts common in the industry. This designation is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device standard

2.1 Description

This 32-bit 1:2 registering clock driver with parity is designed for 1.2 V VDD operation.

All inputs are pseudo-differential with an external or internal voltage reference. All outputs are full swing CMOS drivers optimized to drive single terminated 25..50 Ω traces in DDR4 RDIMM and LRDIMM applications. The clock outputs Yn_t and Yn_c and control net outputs QxCKEn, QxCSn and QxODTn can be driven with a different strength to compensate for different DIMM net topologies. By disabling unused outputs the power consumption is reduced.

The DDR4RCD01 operates from a differential clock (CK_t/CK_c). Inputs are registered at the crossing of CK_t going HIGH, and CK_c going LOW. The input signals could be either re-driven to the outputs or they could be used to access device internal control registers when certain input conditions are met. The control word mechanism is described in more detail in 2.18.2, Control Word Decoding.

2.2 Features and Functions

The DDR4RCD01 has three basic modes of operation associated with the DA[1:0] bits in the DIMM Configuration Control Word (RC0D):

- In **Direct DualCS mode** (DA[1:0] = 00) the component has two chip select inputs, DCS0_n and DCS1_n, and two copies of each chip select output, QACS0_n, QACS1_n, QBCS0_n and QBCS1_n. The inputs pins DC[2:0] are forwarded to two sets of output pins, QAC[2:0] and QBC[2:0]. This is the normal operating mode ("QuadCS disabled" and "Encoded CS disabled").
- In **Direct QuadCS mode** (DA[1:0] = 01), the component has four chip select inputs, the two dedicated inputs DCS[1:0]_n and the DC[0] input pin functioning as DCS2_n and the DC[1] input pin functioning as DCS3_n, and two copies of each chip select output, QACS[3:0]_n and QBCS[3:0]_n. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the "QuadCS enabled" mode.

  In the two modes above the DDR4 register does not need to decode input signals to generate any chip select outputs.
- In **Encoded QuadCS mode** (DA[1:0] = 11), two copies of four output chip selects, i.e., QACS[3:0]_n and QBCS[3:0]_n, are decoded out of two DCS[1:0]_n inputs and the DC[0] input. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the "Encoded QuadCS" mode.

When the DCS encoding is changed (i.e., when the setting in RC0D DA[1:0] is updated), it is necessary for the host to precondition the signals driven on the pins which will be turned into chip select inputs with the correct voltage levels. For example, it is necessary to drive DCS[3:2] both HIGH before RC0D DA[1:0] is updated from '00' to '01'. This is necessary to prevent a violation of the t_{MRD} parameter.