JEDEC STANDARD

DDR4 Data Buffer Defintion (DDR4DB01)

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(From JEDEC Board Ballot JCB-14-12, formulated under the cognizance of the JC-40.4 Subcommittee on Registered & Fully Buffered Memory Support Logic.)

1 Scope

This standard defines standard specifications for features and functionality, DC and AC interface parameters and test loading for definition of the DDR4 data buffer for driving DQ and DQS nets on DDR4 LRDIMM applications. Any TBDs as of this document, are under discussion by formulating committee.

The purpose is to provide a standard for the DDR4DB01 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation DDR4DB01 refers to the part designation of a series of commercial logic parts common in the industry. This designation is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device standard

2.1 Description

This dual 4-bit bidirectional data register with differential strobes is designed for 1.2 V V_{DD} operation. The device has a dual 4-bit host bus interface that is connected to a memory controller and a dual 4-bit DRAM interface that is connected to two x4 DRAMs. It also has an input-only control bus interface that is connected to a DDR4 Register. This interface consists of a 4-bit control bus, two dedicated control signals, a voltage reference input and a differential clock input.

All DQ inputs are pseudo-differential with an internal voltage reference. All DQ outputs are V_{DD} terminated drivers optimized to drive single or dual terminated traces in DDR4 LRDIMM applications. The differential DQS strobes are used to sample the DQ inputs and are regenerated in the DDR4DB01 for driving out the DQ outputs on the opposite side of the device.

The clock inputs BCK_t and BCK_c are used to sample the control inputs BCOM[3:0], BCKE and BODT. The BCOM[3:0] inputs are used to write device internal control registers. The buffer control word (BCW) mechanism is described in more detail in 2.5.

The DDR4DB01 also supports dedicated pins for ZQ calibration and for parity error alerts.

2.1.1 Power-on Initialization

To ensure defined outputs from the register before a stable clock has been supplied, the memory buffer must enter the reset state during power-up. After the voltage ramp, stable power is held for a minimum of 200 µs in the RESET state (i.e., the BCK_t/BCK_c inputs are held LOW and the BCKE input is held HIGH). In the RESET state all other input receivers are disabled, and can be left floating. In the RESET state, all control registers are restored to their default states (which is “0”, except when explicitly defined otherwise). All outputs must float. In the RESET state the data buffer is in low power state and host interface or DRAM interface termination is disabled.

With a falling edge of the BCKE input, the data buffer transitions to the clock stopped power down mode. A certain period of time (t_{ACT}=16 t_{CK}) before the BCKE input is pulled LOW the reference voltage BVrefCA needs to be stable within specification.

With stable clock input signals BCK_t/BCK_c and BCKE still held LOW, the buffer transitions into the equivalent of CKE power down mode.