

JEDEC STANDARD

Inspection Criteria for Microelectronic Packages and Covers

JESD9C

(Revision of JESD9B, May 2011)

MAY 2017

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2017
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

INSPECTION CRITERIA FOR MICROELECTRONIC PACKAGES AND COVERS

Contents

	Page
Foreword	ii
1 Scope	1
2 Normative Reference	1
3 Terms and Definitions	2
4 General Requirements	10
4.1 Quality System	10
4.2 Quality and Screening	10
4.3 Order of Precedence	10
4.4 Optical Inspection Magnification	10
4.5 Controlling Dimension	10
5 Insulator Criteria (Metal Packages: Glass-to-metal and Ceramic-to-metal Seals)	11
5.1 Insulator Bubbles	11
5.2 Insulator Cracks, Chip-outs, Cracking	13
5.3 Insulator Climb, Overflow, Splatter	17
5.4 Other Insulator Conditions	19
6 Braze Criteria (Metal Packages)	21
6.1 Undercut Braze, Non-continuous Braze, Misalignment	21
6.2 Porous and Peeling Braze	22
6.3 Braze Run-out	23
6.4 Braze Climb	24
7 Leads (Metal and Ceramic Packages)	26
7.1 Lead Nicks, Pits, Voids, Indentations, Scratches, Over-etching, Protrusions	26
7.2 Lead Surface Finish	29
7.3 Off-center, Bent, Angled, or Broken Leads	31
8 General Package Criteria (Metal Packages)	34
8.1 Package Nicks, Pits, Voids, Indentations, Scratches, Protrusions, Chip-outs	34
8.2 Package Surface Finish	40
9 General Cover Criteria (Metal Covers)	42
9.1 Cover Nicks, Pits, Voids, Indentations, Scratches, Protrusions, Chip-outs	42
9.2 Cover Surface Finish	45
10 General Package Criteria (Ceramic Packages: Non-metallized Areas)	46
10.1 Ceramic Chip-outs, Cracks, Delamination, Separation, Voiding, Protrusions, Fins	46
11 Metallization Criteria (Ceramic Packages)	50
11.1 General	50
11.2 Contact Pad Metallization	50
11.3 Seal Area Metallization	53
11.4 Bonding Area Metallization	57
11.5 Die Attach Area	61
11.6 Braze Pad Metallization	64
11.7 Castellated Metallization	66
12 Lead Attachment (Ceramic Packages)	67
12.1 Lead to Braze Pad Attachment	67
12.2 Lead to Pad Misalignment	69
Annex A (informative) Index of Figures	70
Annex B (informative) Differences between revisions	73

Foreword

The purpose of this JEDEC standard is to verify the workmanship and requirements of microelectronic packages and covers (lids) intended for use in fabricating hybrid microelectronic circuits / microcircuits (hereafter referred to as “microcircuits”). It is applicable for use by the package manufacturer (i.e., package components), and the microcircuit manufacturer (i.e., from incoming inspection of package components through final inspection of the completed microcircuit).

This standard also encompasses and replaces JESD27, *Ceramic Package Specification for Microelectronic Packages*. It is meant to be used in conjunction, and to not contradict, with MIL-STD-883, Test Method 2009: External Visual. This standard provides the package manufacturer, microcircuit manufacturer, and microcircuit customer a complete set of microelectronic package workmanship inspection requirements.

INSPECTION CRITERIA FOR MICROELECTRONIC PACKAGES AND COVERS

(From JEDEC Board Ballot JCB-11-23 and JCb-17-05, formulated under the cognizance of the JC-13.5 Committee on Hybrid Microcircuit Technology)

1 Scope

This standard establishes the inspection criteria for metal and ceramic hermetic packages, individual feed throughs, and covers (lids).

2 Normative Reference

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

MIL-PRF-38534, *Hybrid Microcircuits, General Specification for*

MIL-PRF-38535, *Microcircuits, General Specification for*

MIL-STD-883, *Test Method Standard, Microcircuits*

Military Standards are available in electronic format from: <http://quicksearch.dla.mil/>.

3 Terms and Definitions

For the purpose of this standard, the terms, definitions, and symbols of MIL-PRF-38534, MIL-PRF-38535, and MIL-STD-883 and the following shall apply and shall be used in the applicable procurement documentation:

- 3.1 annular ring:** The metallization pad area around the top or bottom of a castellation hole.
- 3.2 base:** The bottom main support area of a package.
- 3.3 base metal:** The unplated main metal material of which the metal package, lead, or braze is constructed.
- 3.4 blistering:** Detachment of material from the surface creating a bubble-like shape.
- 3.5 bonding (critical) area:** The surface on a lead or package to which wires will be bonded (i.e., the wirebond area).
- NOTE 1 This term is not to be confused with the “die bond area” which is specified as the “die attach area” in this standard.
- NOTE 2 The critical wire bond area on a ceramic package is a metallization trace whose length is 0.015 inches (0.381 mm) and whose width is 80% of the width of the designed wirebond trace, as specified in the applicable procurement document.
- 3.6 bonding trace; wirebond trace:** A metallized path on a package or substrate to which a bond wire is wirebonded.
- 3.7 braze:** A metallic material used to join two metals or metallized components.
- 3.8 braze climb:** The distance from the surface of the package to the top of the braze line on a lead, not including braze flash.
- 3.9 braze flash:** The braze material that has flowed over or out of the designed contained braze area and is less than 0.001 inches (0.0254 mm) thick.
- 3.10 braze run-out:** The braze material that has flowed over or out of the designed contained braze area, not including braze flash.
- 3.11 braze, undercut:** The braze material recessed from the package surface at the interface of the package wall and the package base.
- 3.12 bubble, subsurface:** A bubble in the glass-to-metal seal that is below the top surface of the seal and is not open or can not be opened with a wood probe.

3 Terms and Definitions (cont'd)

3.13 bubble, surface; open-surface bubble: A bubble in the glass-to-metal seal that is at the top surface of the seal and is either open or can be opened with a wood probe.

3.14 castellation: A semicircular or crown-shaped metallized surface.

3.15 chip-out: An area where a crack has allowed a portion of the insulator to break away leaving a void in the insulator at the metal interface.

3.16 concentric: Having a common center point.

3.17 corrosion: The breaking down or destruction of a material, especially a metal, through a chemical reaction.

NOTE The most common form of corrosion is rusting, which occurs when iron combines with oxygen and water.

3.18 cover: A lid that is soldered, seam-sealed, projection-welded, etc. to the package to create a hermetically sealed microcircuit.

3.19 crack, circumferential: A crack that appears on the surface of an insulator and follows the shape of the package hole.

3.20 crack, meniscus: A crack confined to the meniscus area of the seal above the average low point of the insulator.

3.21 crack, radial: A crack that appears on the surface of the insulator and either starts at the package and extends towards the lead or starts at the lead and extends towards the package propagating past the average low point of the insulator.

3.22 crazing: Multiple minute cracks that appear on the surface of the insulator.

3.23 delamination: The detachment of a sheet-like layer of material from a surface.

3 Terms and Definitions (cont'd)

3.24 die (attach) area: An area of a package used for die placement and typically located on the bottom inside surface of the base of the package.

NOTE For ceramic package cavities, the die attach area is defined as the area that is within a 0.020-inch (0.508-mm) perimeter from the die attach cavity wall (Figure 3.24-1).

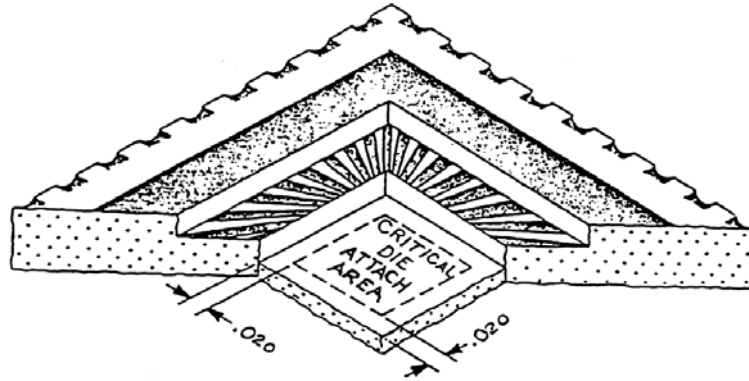


Figure 3.24-1 — Critical die attach area in a ceramic package cavity

3.25 eyelet: A ring of metal used as the outside member of a hermetic lead seal to hold a feed-through in place, typically soldered into the package.

3.26 fin: A fine feather edge protrusion occurring at an edge.

3.27 fin, hanging: A fin that can be moved with a probe but is still connected to the surface.

3.28 flaking: The detachment of a sheet-like layer of material from a surface.

3.29 foreign material: Any adhering material or residue not intentionally added or included in the piece part composition by design.

3.30 heat sink: A heat exchange material, typically metal or ceramic, designed to absorb and dissipate excess heat from one or more devices in a circuit.

3.31 indentation: A notch or deep recess in a surface.

3.32 insulator: A lead seal material (typically matched glass, compression glass, or brazed ceramic) that electrically isolates a lead from the package and creates a hermetic seal.

3.33 insulator climb: The amount of insulator measured from the surface of the package to the top of the insulator line on the lead.