ESDA/JEDEC Joint Standard

ANSI/ESDA/JEDEC JS-001-2017

ANSI/ESDA/JEDEC JS-001-2017
Revision of ANSI/ESDA/JEDEC JS-001-2014

For Electrostatic Discharge Sensitivity Testing

Human Body Model (HBM) - Component Level

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ESD ASSOCIATION® JEDEC®

ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing -

Human Body Model (HBM) - Component Level

Approved December 8, 2016
EOS/ESD Association, Inc. & JEDEC Solid State Technology Association

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FOREWORD

This joint standard was developed under the guidance of the JEDEC JC-14.1 committee on Reliability Test Methods for Packaged Devices and the ESDA Standards Committee. The content was developed by a joint working group composed of members of the JEDEC ESD Task Group and ESDA Working Group 5.1 (Human Body Model). The standard is intended to replace the human body model ESD standard ANSI/ESDA/JEDEC JS-001-2014.

This revision (2017) introduces a new test level at 50 volts and a new classification. These items have been added to address the increasing number of devices with ESD withstand thresholds in the 50 volt region and below. Technical specifications and guidelines for use of attenuators in making discharge current measurements were added. Attenuators are not recommended for the 50- and 125-volt levels since the expected currents are quite low.

Another change added to this revision is an informative Annex (H) which contains some suggested methods for finding "failure windows", voltage ranges where the device may fail even though it passes at higher levels. While these failure windows are rare, these methods were added so that an accepted approach could be used to demonstrate whether the windows exist in a given case.

The section on safe ESD handling was modified to include citations of the most commonly used ESD control standards. "Threshold" was added to the ESD withstand voltage definition to be consistent with terminology used in the body of the standard. Various typographical errors were also fixed.

This standard is maintained and revised as a joint standard through a Memorandum of Understanding between JEDEC and ESDA. This standard is a living document and revisions and updates will be made on a routine basis driven by the needs of the electronic industry.

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At the time ANSI/ESDA/JEDEC JS-001-2017 was prepared, the Joint HBM Subcommittee had the following members:

The following individuals contributed to the development of ANSI/ESDA/JEDEC JS-001-2014, ANSI/ESDA/JEDEC JS-001-2012, ANSI/ESDA/JEDEC JS-001-2011, and ANSI/ESDA/JEDEC JS-001-2010.

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1.0 SCOPE AND PURPOSE

1.1 Scope

This standard establishes the procedure for testing, evaluating, and classifying components and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined human body model (HBM) electrostatic discharge (ESD).

1.2 Purpose

The purpose (objective) of this standard is to establish a test method that will replicate HBM failures and provide reliable, repeatable HBM ESD test results from tester to tester, regardless of component type. Repeatable data will allow accurate classifications and comparisons of HBM ESD sensitivity levels.

1.2.1 Existing Data

Data previously generated with testers meeting all waveform criteria of ANSI/ESDA/JEDEC JS-001-2010 and subsequent versions, ANSI/ESD STM5.1-2007, or JESD22-A114F shall be considered valid test data.

2.0 REFERENCES

ESD ADV1.0, ESD Association's Glossary of Terms[1]

JESD99, JEDEC Standard - Terms, Definitions, and Letter Symbols for Microelectronic Devices[2]

2.1 Other Documents

ANSI/ESD STM5.1-2007, ESD Association Standard Test Method for Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) Component Level[1]

JESD22 – A114F, December 2008, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)[2]

3.0 DEFINITIONS

The terms used in the body of this document are in accordance with the definitions found in ESD ADV1.0, ESD Association's Glossary of Terms and JESD99 JEDEC Standard –Terms, Definitions, and Letter Symbols for Microelectronic Devices. Terms separated by a semicolon (;) are considered to be synonyms. In this document the term "pin" is used to represent any device pin, land, bump, ball, or die pad.

above-passivation layer (APL). A low-impedance metal plane, built on the surface of a die above the passivation layer that connects a group of bumps or pins (typically power or ground).

NOTE: This structure is sometimes referred to as a redistribution layer (RDL). There may be multiple APLs (sometimes referred to as islands) for a power or ground group.

associated non-supply pin. A non-supply pin (typically an input, output or I/O pin) is associated with a supply pin group if either:

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- the current from the supply pin group (i.e., VDDIO) is required for the function of the electrical circuit(s) (I/O driver) that connect (high/low impedance) to that non-supply pin; or
- a parasitic path exists between non-supply and supply pin group (e.g., open-drain type non-supply pin to a VCC supply pin group that connects to a nearby N-well guard ring).

cloned non-supply (IO) pin. Any of a set of input, output, or bidirectional pins using the same IO cell and electrical schematic and sharing the same associated supply pin group(s) including ESD power clamp(s).

component. An item such as a resistor, diode, transistor, integrated circuit or hybrid circuit.

NOTE: A component may also be referred to as a device.

component failure. A condition in which a tested component does not meet one or more specified static or dynamic data sheet parameters.

coupled non-supply pin pair. Two pins, such as differential amplifier inputs, or low-voltage differential signaling (LVDS) pins, that have between them an intended direct current path, such as a pass gate or resistor.

NOTE: These pairs include analog and digital differential pairs and other special function pairs (e.g., D+/D-, XTALin/XTALout, RFin/RFout, TxP/TxN, RxP/RxN, CCP_DP/CCN_DN etc.).

data sheet parameter. Any of the static and dynamic component performance data supplied by the component manufacturer or supplier in a data sheet or other product specification.

dynamic parameter. A parameter measured with the component in an operating condition.

NOTE: These may include, but are not limited to full functionality, output rise and fall times under a specified load condition, and dynamic current consumption.

ESD withstand voltage; withstand threshold. The highest voltage level that does not cause device failure with the device passing all tests performed at lower voltages.

NOTE: See note under “failure window” definition.

exposed pad. An exposed metal plate on an IC package, connected to the silicon substrate and acting as a heat sink.

NOTE 1: This metal plate may or may not be electrically connected to the die.

NOTE 2: The exposed pad may be categorized as either supply, non-supply or no-connect.

failure window. An intermediate range of stress conditions that can induce failure in a particular device type while the device type can pass some stress conditions both higher and lower than this range.

NOTE: For example, a component with a failure window may pass a 500-volt test, fail a 1000-volt test and pass a 2000-volt test. Hence, the failure window of the device is between 500 volts and 2000 volts. The withstand voltage of this device is 500 volts.

feedthrough. A direct or indirect (via a series resistor) connection from a pad cell layout that can allow additional elements, not included in the pad cell, to make electrical connections to the bond pad. (See Annex G.)

NOTE: This is not to be confused with the term feedthrough used in Section 5.0 which refers to test boards.

HBM ESD tester; HBM simulator. Equipment that applies a human body model (HBM) ESD to a component.

NOTE: This equipment is also referred to as “tester” in this standard.

human body model (HBM) ESD. An electrostatic discharge (ESD) event meeting the waveform criteria specified in this standard, approximating the discharge from the fingertip of a typical human being to a grounded device.

Ips (peak current value). The current value determined by linear extrapolation of the exponential current decay curve back to the time (t_{max}) when the current actually peaked (Ips_{max}).

NOTE: The linear extrapolation should be based on the current waveform data over a 40-nanosecond period beginning at t_{max}. (See Figure 2A.)

Ips_{max} (peak current maximum value). The highest current value measured.

NOTE: This value includes the overshoot or ringing components due to internal test simulator RLC parasitics. (See Figure 2A.)

no-connect pin. A package interconnect (pin, bump, or ball) that is not electrically connected to a die.

NOTE: In practice, there are some pins that are labeled as "no-connect", but that are actually connected to the die and, therefore, should not be classified as a no-connect pins for the purpose of ESD testing.

non-socketed tester. An HBM simulator that makes contact to the device under test (DUT) pins (or balls, lands, bumps, or die pads) with test probes rather than placing the DUT in a socket.

non-supply pin. A pin that is not categorized as a supply pin or a no-connect.

NOTE: Non-supply pins include pins such as input, output, offset adjusts, compensation, clocks, controls, address, data, Vref pins and VPP pins on EPROM memory. Most non-supply pins transmit or receive information such as digital or analog signals, timing, clock signals, and voltage or current reference levels.

package plane. A low-impedance metal layer built into an IC package connecting a group of bumps or pins (typically power or ground). There may be multiple package planes (sometimes referred to as islands) for each power and ground group.

pre-pulse voltage. A voltage occurring at the device under test (DUT) just prior to the generation of the HBM current pulse. (See Annex B.2.)

pulse generation circuit. The circuit network that produces a human body discharge current waveform.

NOTE: The circuit network includes a pulse generator with its test equipment internal path up to the contact pad of the test fixture.

NOTE: This circuit is also referred to as a dual-polarity pulse source.

ringing. A high-frequency oscillation superimposed on a waveform.

shorted non-supply pin. Any non-supply pin (typically an input, output or I/O pin) that is metallically connected (typically < 3 ohm) on the chip or within the package to another non-supply pin (or set of non-supply pins).

socketed tester. A simulator that makes contact to DUT pins (or balls, lands, bumps, or die pads) using a DUT socket mounted on a test fixture board.

specification limit (SPL). The HBM limit value set by customer requirement or internal target. (See Annex G.)

spurious current pulse. A small HBM shaped pulse that follows the main current pulse and is typically defined as a percentage of Ips_{max}.

supply pin. Any device pin that provides operating current to that device.

NOTE: Supply pins typically transmit no information (such as digital or analog signals, timing, clock signals, and voltage or current reference levels). For the purpose of ESD testing, power and ground pins are treated as supply pins.

static parameter. A parameter measured with the component in a non-operating condition.

NOTE: Static parameters may include, but are not limited to, input leakage current, input breakdown voltage, output high and low voltages, output drive current, and supply current.

step-stress-test hardening. The process of increasing the ESD withstand threshold by applying stress incrementally from low voltage to higher values.

NOTE: This hardening occurs when a component subjected to increasing ESD voltage step-stresses is able to withstand higher stress levels than when another component expected to have the same threshold is evaluated using no step-stressing.

NOTE: For example: a component may fail at 1000 volts if subjected to a single stress, but fail at 3000 volts if stressed incrementally from 250 volts.

test fixture board. A specialized circuit board, with one or more component sockets, that connects the DUT(s) to the HBM simulator.

t_{max}. The time when the current is at its maximum value (Ips_{max}). (See Figure 2A.)

trailing current pulse. A current pulse that occurs after the HBM current pulse has decayed. (See Annex B.1.)

NOTE: A trailing current pulse is a relatively constant current often lasting for hundreds of microseconds.

two-pin tester. A low-parasitic HBM simulator that tests DUTs in pin pairs in which floating pins are not connected to the simulator, thereby eliminating DUT-tester interactions from parasitic tester loading of floating pins.

V1. The maximum HBM stress voltage step at which all of the selected cloned non-supply pins pass. (See Annex G.)

V2. The minimum HBM stress voltage step at which all the selected cloned non-supply pins fail. (See Annex G.)

VM. The minimum HBM stress voltage step at which 50% or greater of the selected cloned non-supply pins fail. (See Annex G.)

4.0 APPARATUS AND REQUIRED EQUIPMENT

4.1 Waveform Verification Equipment

All equipment used to evaluate the tester shall be calibrated in accordance with the manufacturer's recommendation. This includes the oscilloscope, current transducer and high-voltage resistor load. Maximum time between calibrations shall be one year. Calibration shall be traceable to national standards, such as the National Institute of Standards and Technology (NIST) in the United States, or comparable international standards.

Equipment capable of verifying the pulse waveforms defined in this standard test method includes, but is not limited to, an oscilloscope, evaluation loads and a current transducer.

4.1.1 Oscilloscope

A digital oscilloscope is recommended but analog oscilloscopes are also permitted. In order to insure accurate current waveform capture, the oscilloscope shall meet the following requirements:

a. Minimum sensitivity of 100 milliamperes per major division when used in conjunction with the current transducer specified in Section 4.1.2.
b. Minimum bandwidth of 350 MHz.
c. For analog scopes, minimum writing rate of one major division per nanosecond.

4.1.1.1 Additional Requirements for Digital Oscilloscopes

a. Recommended channels: 2 or more
b. Minimum sampling rate: 1 GS/s
c. Minimum vertical resolution: 8-bit
d. Minimum vertical accuracy: + 2.5%
e. Minimum time base accuracy: 0.01%
f. Minimum record length: 10 k points

4.1.2 Current Transducer (Inductive Current Probe)

a. Minimum bandwidth of 200 MHz.
b. Peak pulse capability of 12 amperes.
c. Rise time of less than 1 nanosecond.
d. Capable of accepting a solid conductor as specified in Section 4.1.3.
e. Provides an output voltage per signal current as required in Section 4.1.1.
   (This is usually between 1 and 5 millivolts per milliampere.)
f. Low-frequency 3-dB-point below 10 kHz (e.g., Tektronix CT2) for measurement of decay constant t_d (see Section 5.2.3.1, Table 1, and note below).

NOTE: Results using a current probe with a low-frequency 3-dB-point of 25 kHz (e.g., Tektronix CT1) to measure decay constant t_d are acceptable if t_d is found to be between 130 and 165 nanoseconds.