JEDEC STANDARD

Temperature, Bias, and Operating Life

JESD22- A108F

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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TEST METHOD A108E
TEMPERATURE, BIAS, AND OPERATING LIFE

(From JEDEC Board Ballots JCB-99-89, JCB-99-89A, JCB-05-49, JCB-10-60, JCB-16-47, and JCB-17-20 formulated under the cognizance of JC-14.1 Committee on Reliability Test Methods for Packaged Devices.)

1 Scope

This test is used to determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way, and is primarily for device qualification and reliability monitoring. A form of high temperature bias life using a short duration, popularly known as burn-in, may be used to screen for infant mortality-related failures. The detailed use and application of burn-in is outside the scope of this document.

1.1 Applicable documents

JESD47, *Stress-Test Driven Qualification of Integrated Circuits*

JEP122, *Failure Mechanism and Models for Silicon Semiconductor Devices*

2 Apparatus

The performance of this test requires equipment that is capable of providing the particular stress conditions to which the test samples will be subjected.

2.1 Circuitry

The circuitry through which the samples will be biased must be designed with several considerations:

2.1.1 Device schematic

The biasing and operating schemes must consider the limitations of the device and shall not overstress the devices or contribute to thermal runaway.

2.1.2 Power

The test circuit should be designed to limit power dissipation such that, if a device failure occurs, excessive power will not be applied to other devices in the sample.

2.2 Device mounting

Equipment design, if required, shall provide for mounting of devices to minimize adverse effects while parts are under stress, (e.g., improper heat dissipation).

2 Apparatus (cont'd)

2.3 Power supplies and signal sources

Instruments (such as DVMs, oscilloscopes, etc.) used to set up and monitor power supplies and signal sources shall be calibrated and have good long-term stability.

2.4 Environmental chamber

The environmental chamber shall be capable of maintaining the specified temperature within a tolerance of ± 5 °C throughout the chamber while parts are loaded and unpowered.

3 Definitions

3.1 Maximum operating voltage

The maximum supply voltage at which a device is specified to operate in compliance with the applicable device specification or data sheet.

3.2 Absolute maximum rated voltage

The maximum voltage that may be applied to a device, beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology.

3.3 Absolute maximum rated junction temperature

The maximum junction temperature of an operating device, beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology.

NOTE Manufacturers may also specify maximum case temperatures for specific packages.

4 Procedure

The sample devices shall be subjected to the specified or selected stress conditions for the time and temperature required.

4.1 Stress duration

The bias life duration is intended to meet or exceed an equivalent field lifetime under application use conditions. The duration is established based on the acceleration of the stress (see JEP122). The stress duration is specified by application qualification requirements, JESD47 or the applicable procurement document. Interim measurements may be performed as necessary per restrictions in clause 6.

4 Procedure (cont'd)

4.2 Stress conditions

The stress condition shall be applied continuously (except during interim measurement periods). The time spent elevating the chamber to accelerated conditions, reducing chamber conditions to room ambient, and conducting the interim measurements shall not be considered a portion of the total specified test duration.

4.2.1 Ambient temperature

The ambient temperature and bias for high temperature stress shall be adjusted to result in a minimum junction temperature of the devices under stress of 125 °C unless otherwise specified as for extended use or other environments. Unless otherwise specified, the ambient temperature for low temperature stress shall be a maximum of –10 °C. For products which experience temperature variations during high temperature stress, it is acceptable to use higher or lower junction temperatures for specified blocks/dynamic stress patterns as long as application lifetime equivalent stress duration targets are achieved.

Note: Devices designed for use in an extended temperature environment may be stressed at temperatures which may extend up to 250°C. The stress temperature may exceed the operating temperature but not the absolute maximum rated temperature and voltage of the technology.

4.2.2 Operating voltage

Unless otherwise specified, the operating voltage should be the maximum operating voltage specified for the device unless the conditions of 4.2.1 cannot be met. A higher voltage is permitted in order to obtain lifetime acceleration from voltage as well as temperature; this voltage must not exceed the absolute maximum rated voltage for the device, and must be agreed upon by the device manufacturer.

4.2.3 Biasing configurations

Biasing configurations may be bias stress (static or pulsed) or operating stress (dynamic). Depending upon the biasing configuration, supply and input voltages may be grounded or raised to a maximum potential chosen to ensure a stressing temperature not higher than the maximum-rated junction temperature. Device outputs may be unloaded or loaded, to achieve the specified output voltage level. If a device has a thermal shutdown feature it shall not be biased in a manner that could cause the device to go into thermal shutdown.

4.2.3.1 High temperature forward bias (HTFB)

The HTFB test is configured to forward bias major power handling junctions of the device samples. The devices may be operated in either a static or a pulsed forward bias mode. Pulsed operation is used to stress the devices at, or near, maximum-rated current levels. The particular bias conditions should be determined to bias the maximum number of the solid state junctions in the device. The HTFB test is typically applied on