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DDR4 PROTOCOL CHECKS

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Contents

Foreword

The intended use of this document is for the validation and debug of DDR4 based designs. This document contains protocol checks, sometimes referred to as memory access rules or protocol violations. These protocol checks can be implemented in simulation for pre-silicon verification or implemented in a protocol analyzer, logic analyzer, or oscilloscope for post silicon verification. The contained list of protocol checks is by no means the definitive list of protocol checks as other checks not contained in this list probably do exist.

This document was created by the JC-40.5 JEDEC Committee. This document is subservient to the JEDEC JESD79-4B DDR4 Specification and the SPD Specification, JESD 21-C Section Title: Annex L: Serial Presence Detect (SPD) for DDR4 SDRAM Modules.

DDR4 PROTOCOL CHECKS

(From JEDEC Board Ballot JCB-17-17, formulated under the cognizance of the JC-40.5 Subcommittee on Logic Validation and Verification.)

1 Scope

This document contains a list of checks that can be used during the verification or debug stages of development to check that accesses to a DDR4 DRAM adhere to JESD79-4B. These checks are derived from JESD79-4B. The intent of this document is not to supplant the JESD79-4B document, but to help consolidate the checks into a single easy to read document. This document was not intended to indicate *how* a protocol check measurement would be made, but *what* measurement would be made. The how can differ based on the testing requirements or the equipment at hand. This document is not a definitive list as other DDR4 protocol checks do exist and can be added to this document during subsequent revisions.

2 Normative reference

JESD79-4B, *DDR4 SDRAM Standard.*

3 Terms and definitions

For the purposes of this document, the following terms and definitions are used in this document.

Symbol: A shorthand notation per JESD79-4B for the Parameter.

NOTE Where the cell is grayed out, there is no official JEDEC parameter currently defined. However the equation is defined.

Parameter: A text description from JESD79-4B describing the time between events targeting the DDR4 DRAM.

Violation Criteria: in formula format is derived from the JESD79-4B specification. This is the protocol check. It is written such that if the condition is satisfied the protocol check fails and a violation exists.

Reference: A guide to the reader of where to look in JESD79-4B for more information on this protocol check. By no means is the reference exhaustive as the Parameter may be listed in many places. This is meant to be a starting point for the reader.

Units: How the protocol check will be measured.

Notes: Guidance as to special cases that concern that particular check and can be found in JESD79-4B.

4 DDR4 Protocol Checks – based on Timing between events

In general, the DDR4 specification details commands and the allowable time between those commands targeted to the DDR4 DRAM. Generally speaking, those commands cannot be too close or too far apart in time. A protocol check is the measurement to ensure that this is adhered to.

Parameter	Symbol	Violation Criteria (Formula)	Reference	Units	Notes
Read to Read Same Bank Group Write to Write Same Bank Group MPR page x to MPR page x (where x = 1,2 or 3)	tCCD_L	Measurement is less than tCCD_Lmin. tCCD_Lmin = MAX(tCCD_L{nCK}, ROUNDUP((tCCD_L{ns}/tCK{ns}) -.025))	Table 14, Table 132, Table 133, Figure 60, Figure 61, Section 4.10.3, 4.25.7	nCK	1,4
Read to Read Different Bank Group Write to Write Different Bank Group MPR page 0 to MPR page 0	tCCD_S	Measurement is less than tCCD_Smin.	Table 132, Table 133, Figure 60, Figure 61, Figure 82, Figure 83, Figure 117, Figure 118, Section 4.10.3, 4.25.7	nCK	1
Read to Write Same Bank Group Read to Write Different Bank Group		Measurement is less than CL - CWL + RBL/2 +1tCK + tWPRE	Section 4.25.6, Figure 84	nCK	1,3
Write to Read Same Bank Group		Measurement is less than CWL + WBL/2 + MAX(tWTR_L{nCK}, ROUNDUP((tWTR_L{ns}/tCK{nS}) -.025))	Section 4.25.6, Table 132, Table 133, Figure 65	nCK	1,3,4
Write to Read Different Bank Group		Measurement is less than CWL + WBL/2 + MAX(tWTR_S{nCK}, ROUNDUP((tWTR_S{nS}/tCK{nS}) -.025))	Section 4.25.6, Table 132 and Table 133, Figure 64	nCK	1,3,4
Activate to Activate Same Bank Group	tRRD_L	Measurement is less than tRRD_Lmin. tRRD_Lmin = MAX(tRRD_L{nCK}, ROUNDUP((tRRD_L{ns}/tCK{nS}) -.025))	Table 132, Table 133, Figure 62	nCK	1,2,4
Activate to Activate Different Bank Group	tRRD_S	Measurement is less than tRRD_Smin. tRRD_Smin = MAX(tRRD_S{nCK}, ROUNDUP((tRRD_S{ns}/tCK{ns}) -.025))	Table 132,133, Figure 62	nCK	1,2,4
Greater than 4 Activate commands window	tFAW	Measurement is less than tFAWmin. tFAWmin = MAX(tFAW{nCK}, ROUNDUP((tFAW{ns}/tCK{ns})-.025))	Table 132, Table 133, Figure 63	nCK	1,2,4