JEDEC STANDARD

Byte Addressable Energy Backed Interface

JESD245B

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BYTE ADDRESSABLE ENERGY BACKED INTERFACE

(From JEDEC Board Ballot JCB-17-15, formulated under the cognizance of the JC-45.6 Subcommittee on Hybrid Modules.)

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FOREWORD

This standard has been prepared by JEDEC. The purpose of this standard is definition of a byte addressable energy backed function on a non-volatile dual in-line memory module (NVDIMM). This standard defines the feature set and commands implemented by the byte addressable energy backed function on an NVDIMM-N.

INTRODUCTION

An NVDIMM-N is a memory module that can be integrated into a standard platform. A Byte Addressable Energy Backed Function on a NVDIMM is designed to preserve data in the event of the power failure. A Byte Address Energy Backed Function is backed by a combination of SDRAM and non-volatile memory (e.g., NAND flash) on the NVDIMM-N. It operates at SDRAM speeds and provides persistent storage by backing up the SDRAM contents into the non-volatile memory in the event of a power failure. This is made possible by an Energy Source (e.g., supercapacitor) which maintains charge on the module enabling back-up of data from SDRAM to the non-volatile memory, providing a storage-class memory solution.

To be able to provide interoperability and the ability for platform and platform software (e.g., BIOS) to support NVDIMM-Ns from various manufacturers, standardization of the host to module interface, discovery mechanism, the feature set and command operations are required, as described in this standard.

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1 SCOPE

This standard specifies the host and device interface for a DDR4 NVDIMM-N, which is a DIMM that achieves non-volatility by copying SDRAM contents into non-volatile memory (NVM) when host power is lost using an Energy Source managed by either the module or the host.

Although this standard is targeted towards DDR4 NVDIMM only, it does not preclude adoption of this standard by other implementations (e.g., DDR3 NVDIMM).

2 NORMATIVE REFERENCES

The normative documents listed in this clause contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

JESD21C, 4.20.28 *DDR4 SDRAM Registered DIMM Design Specification*, Revision 1.00 (August 2015)

JESD21C, 4.1.2.L-4 *Annex L: Serial Presence Detect (SPD) for DDR4 SDRAM Modules* (DDR4 SPD Document Release 4)

JESD21C, 4.1.2.L-5 *Annex L: Serial Presence Detect (SPD) for DDR4 SDRAM Modules* (DDR4 SPD Document Release 5)(forthcoming)

JESD21C, 4.1.6 *Definitions of the EE1004-v 4 Kbit Serial Presence Detect (SPD) EEPROM and TSE2004av 4 Kbit SPD EEPROM with Temperature Sensor (TS) for Memory Module Applications*

JESD21C, 4.1.6-2 *Definitions of the EE1004av 4 Kbit Serial Presence Detect (SPD) EEPROM and TSE2004av 4 Kbit SPD EEPROM with Temperature Sensor (TS) for Memory Module Applications* (forthcoming)

JESD79-4A, *DDR4 SDRAM* (November 2013)

JESD79-4B, *DDR4 SDRAM* (June 2017)

JESD82-31, *DDR4 Registering Clock Driver – DDR4RCD01* (August 2016)

JESD82-31A, *DDR4 Registering Clock Driver – DDR4RCD02* (forthcoming)

JESD82-32, *DDR4 Data Buffer* – DDR4DB01 (August 2016)

JESD82-32A, *DDR4 Data Buffer* – DDR4DB02 (forthcoming)

JESD245, *Byte Addressable Energy Backed Interface* (December 2015)

JESD245A, *Byte Addressable Energy Backed Interface* (September 2016)

JESD248 *DDR4 NVDIMM-N Design Specification* (Revision 1.0)(September 2016)

JESD248A *DDR4 NVDIMM-N Design Specification* (forthcoming)

I^2C Bus Specification Revision 6 (4 April 2014)

System Management Bus (SMBus) Specification Version 3.0 (20 December 2014)

3 TERMS AND DEFINITIONS

For the purposes of this standard, the terms and definitions given in the document included in clause 2 “Normative References” and this clause apply.

3.1 Acronyms

DDR3	Double Data Rate version 3
DDR4	Double Data Rate version 4
DIMM	Dual In-line Memory Module
ES	Energy Source
I^2C	Inter IC (inter integrated circuit)
LCOM	LCOM Bus
NVDIMM	Non-volatile Dual In-line Memory Module
NVDIMM-N	NVDIMM with a Byte Addressable Energy Backed Interface function
NVM	Non-Volatile Memory
NVRDIMM-N	NVDIMM-N that is an RDIMM
RCD	Registering Clock Driver
RDIMM	Registered DIMM
SDRAM	Synchronous Dynamic Random Access Memory
SMBus	System Management Bus
SPD	Serial Presence Detect

3.2 Terms and Definitions

Abort: Operation that stops the currently running operation on the module. See 0.

Arm: Operation that enables or disables trigger(s) for a Catastrophic Save operation. See 7.2.4.

Catastrophic Save: Operation that copies the SDRAM contents into NVM when power is lost. The Catastrophic Save operation is started when an enabled trigger occurs or a write to an I^2C register occurs. See 7.2.1.

CKE Power Down mode: RCD mode in which all input buffers are disabled except for CK_t/CK_c, DCKEn, DRST_n, and sometimes DODTn and ERROR_IN_n. See JESD82-31A (DDR4RCD02).

Clock Stopped Power Down mode: RCD mode in which all input buffers are disabled except for CK_t/CK_c. See JESD82-31A (DDR4RCD02).

Device Managed Policy: Energy Source policy where the module manages the Energy Source used during the Catastrophic Save operation.

Energy Source: A device that is capable of storing and providing energy to the module during a Catastrophic Save operation. See 0.

Erase: Operation that deletes the previously saved SDRAM image in NVM. See 0.

Factory Default: Operation that erases all NVM on the module and resets readable registers to their factory default values except the data needed to determine warranty compliance. This operation does not impact firmware on the module. See 7.2.9.

Firmware Operations: Operations that are related to updating the firmware on the module. See 0.

Host: The system in which the module is installed.

Host Managed Policy: Energy Source policy where the host manages the Energy Source used during the Catastrophic Save operation.

I^2C Bus: A bidirectional 2-wire bus for efficient inter-IC control.

LCOM: A local communication bus, bidirectional 6-wire interface that connects the module's controller to other components.

Management Operations: Operations that either reset the controller or clear status register(s). See 7.2.5.

Maximum Power Saving mode: SDRAM mode similar to Self-Refresh mode that does not perform internal refreshes. See JESD79-4B (DDR4 SDRAM).

Power Down mode: SDRAM mode in which all input buffers except CK_t/CK_c, CKE, RESET_n, and sometimes ODT are disabled. See JESD79-4B (DDR4 SDRAM).

Restore: Operation that restores previously saved SDRAM contents from NVM to SDRAM. See 7.2.2.

RCD Control Words: The registers on a RDIMM that configure the RCD for operational use.

Saturating counter: a counter that remains at its maximum value after reaching its maximum value

Self-Refresh mode: SDRAM mode in which all input buffers except CKE and RESET_n are disabled. See JESD79-4B (DDR4 SDRAM).

SDRAM Mode Registers: The registers on SDRAM that configure the SDRAM for operational use. Some of the mode registers are write-only registers.

Set Energy Source Policy: Operation that configures the Energy Source to be used by the module in the Catastrophic Save operation. See 7.2.6.

Set Event Notification: Operation that either enables or disables notification support on the module when certain events occur. See 7.2.7.

Typed Block Data: A collection of data that is transferred between the host and module in 32 byte blocks. See 5.4.

Vendor Log Page: An optional area on the module that is accessible by the host and containing vendor specific data useful to triage issues on the module. See 7.12.

3.3 Keywords

Several keywords are used to differentiate levels of requirements and options, as follow:

Can - A keyword used for statements of possibility and capability, whether material, physical, or causal (*can* equals *is able to*).

Expected - A keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

Ignored - A keyword that describes bits, bytes, quadlets, or fields whose values are not checked by the recipient.

Mandatory - A keyword that indicates items required to be implemented as defined by this standard.

May - A keyword that indicates a course of action permissible within the limits of the standard (*may* equals *is permitted*).

Must - The use of the word *must* is deprecated and shall not be used when stating mandatory requirements; *must* is used only to describe unavoidable situations.

Optional - A keyword that describes features which are not required to be implemented by this standard. However, if any optional feature defined by the standard is implemented, it shall be implemented as defined by the standard.

Reserved - A keyword used to describe objects—bits, bytes, and fields—or the code values assigned to these objects in cases where either the object or the code value is set aside for future standardization. Usage and interpretation may be specified by future extensions to this or other standards. A reserved object shall be zeroed or, upon development of a future standard, set to a value specified by such a standard. The recipient of a reserved object shall not check its value. The recipient of a defined object shall check its value and reject reserved code values.

Shall - A keyword that indicates a mandatory requirement strictly to be followed in order to conform to the standard and from which no deviation is permitted (*shall* equals *is required to*). Designers are required to implement all such mandatory requirements to assure interoperability with other products conforming to this standard.

Should - A keyword used to indicate that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is deprecated but not prohibited (*should* equals *is recommended that*).

Will - The use of the word *will* is deprecated and shall not be used when stating mandatory requirements; *will* is only used in statements of fact.

3.4 Conventions

This standard uses the conventions described in this subclause.

A binary number is represented in this standard by any sequence of digits consisting of only the Western-Arabic numerals 0 and 1 immediately followed by a lower-case b (e.g., 0101b). Spaces may be included in binary number representations to increase readability or delineate field boundaries (e.g., 0 0101 1010b).

A hexadecimal number is represented in this standard by any sequence of digits consisting of only the Western-Arabic numerals 0 through 9 and/or the upper-case English letters A through F immediately followed by a lower-case h (e.g., FA23h). Spaces may be included in hexadecimal number representations to increase readability or delineate field boundaries (e.g., B FD8C FA23h).

A decimal number is represented in this standard by any sequence of digits consisting of only the Western-Arabic numerals 0 through 9 not immediately followed by a lower-case b or lower-case h (e.g., 25).

A range of numeric values is represented in this standard in the form "a to z", where a is the first value included in the range, all values between a and z are included in the range, and z is the last value included in the range (e.g., the representation "0h to 3h" includes the values 0h, 1h, 2h, and 3h).

When the value of the bit or field is not relevant, x or xx appears in place of a specific value.

4 INTRODUCTION

A nonvolatile DIMM (NVDIMM) is a DIMM that maintains the contents of SDRAM during power loss. An NVDIMM-N achieves non-volatility by:

- performing a Catastrophic Save operation to copy SDRAM contents into NVM when host power is lost using an Energy Source managed by either the module or the host; and
- performing a Restore operation to copy contents from the NVM to SDRAM when power is restored.

This standard defines an I^2C Bus-based register interface for a NVDIMM-N called the Byte Addressable Energy Backed Interface. Figure 1 shows the components of an NVDIMM-N that differ from a regular DIMM. The Non-Volatile Memory Subsystem Controller (i.e., the controller) includes a memory controller for the SDRAM, an NVM controller for the NVM, and I^2C registers. The NVDIMM-N draws power for the Catastrophic Save operation either from the host via the V_12 pin or from a Device-Managed Energy Source.

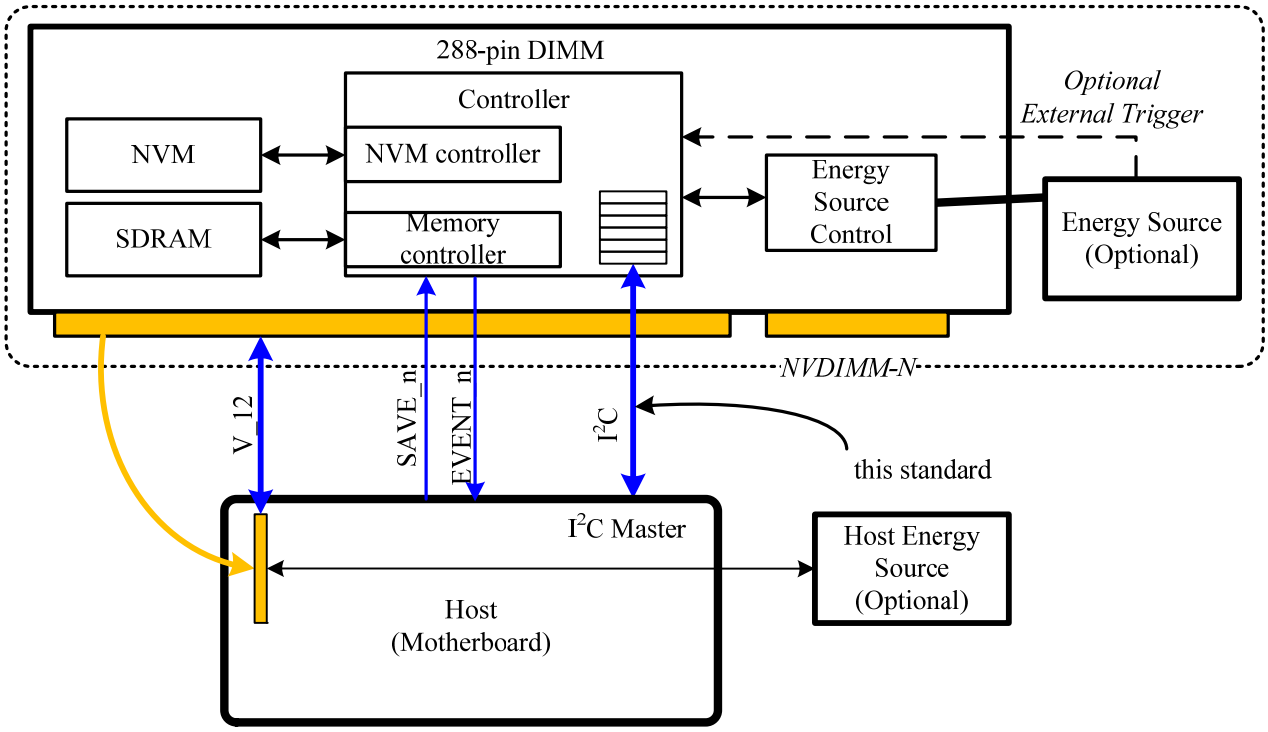

Figure 1 — NVDIMM-N overview