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Constant-Temperature Aging Method to Characterize Copper Interconnect Metallization for Stress-Induced Voiding

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CONSTANT-TEMPERATURE AGING METHOD TO CHARACTERIZE COPPER INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING

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CONSTANT-TEMPERATURE AGING METHOD TO CHARACTERIZE COPPER INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING

(From JEDEC Board Ballot JCB-15-06, formulated under the cognizance of the JC-14.2 Committee on Wafer-Level Reliability.)

1 Scope

This document describes a constant temperature (isothermal) aging method for testing copper (Cu) metallization test structures on microelectronics wafers for susceptibility to stress-induced voiding (SIV). This method is to be conducted primarily at the wafer level of production during technology development, and the results are to be used for lifetime prediction and failure analysis. Under some conditions, the method may be applied to package-level testing. This method is not intended to check production lots for shipment, because of the long test time.

Dual damascene Cu metallization systems usually have liners, such as tantalum (Ta) or tantalum nitride (TaN) on the bottom and sides of trenches etched into dielectric layers. Hence, for structures in which a single via contacts a wide line below it, a void under the via can cause an open circuit at almost the same time as any percentage resistance shift that would satisfy a failure criterion.

The method assumes that void growth (and therefore resistance changes) can be modeled as described by Ogawa, et al.[1], Yao, et all [2, 3] Fischer et al. [5,6], to obtain a median lifetime, an effective activation energy, and an acceleration factor for lifetime.

2 Stress induced voiding in copper

2.1 Stress-induced voids

Stress migration (SM) or stress-induced-voiding (SIV) is one of the key aspects of Cu interconnect technology reliability qualification. The SIV damages are caused by the stress gradient as driving force through the means of diffusion. For Cu interconnects, it is known qualitatively that the intrinsic SIV risk is higher for a wide line relatively to a narrow line structure with a fixed single via size [1-4, 7-11]. As industrial standards, SM reliability data have been treated qualitatively to define pass or fail criteria. The agreed guard-band of “zero fails during a fixed time period” as SM qualification passing criteria has been generally accepted by the industry [8]. This approach was inherited from Al SIV testing method for Cu SIV guard-band but with certain degrees of uncertainty. With the further technology scaling, the Cu SIV reliability margin becomes narrower. Therefore, the old traditional standard could lead to even larger error bars for reliability projections. In order to overcome this known trend of increasing SIV risk, a quantitative SIV lifetime estimation method is needed.

2.1 Stress-induced voids (cont'd)

In recent years, the SIV mechanism has been investigated to reduce SIV risk and established SM qualification methodology [1-4, 7]. Due to the improvement of integration process, progress has been made in SM reliability performance in meeting the design lifetime goals. In general, observation of SM fails is not expected for design rule compliant (DRC) linewidth structures even at the worst temperatures during SM reliability testing period (i.e., 500 h to 1000 h). It is possible to measure SM fails from reasonable wide linewidth test structures within reasonable testing period of time. In [2,3], a geometry linewidth dependent factor was introduced to support an SM model for lifetime extrapolation. The quantified linewidth dependent SM data from 45 nm, 32 nm, and 28 nm show a common power-law factor M. This further supports the SM model with a geometry linewidth factor for acceleration [2,3]. In this spec, in addition to the traditional method, we will apply the SM lifetime model and the equation to develop an SM reliability qualification methodology for meeting the product design lifetime.

2.2 Stress temperature

Cu SM data show a strong temperature dependence of SM lifetime. Based on the Creep voiding rate model by McPherson & Dunn [1, 2, 3, 16,17], we have the median time-to-fail (MTF) relationship:

$$MTF = A(T_0 - T)^{-N} \exp(E_A / k_B T) \tag{1}$$

where T_0 is the stress-free temperature at which the thermomechanical stress transits from tensile to compressive, N is the thermal stress component, E_A is the diffusion activation energy, k_B is the Boltzmann constant and A is normalization constant.

As an example, Figure 1 shows the MTF distribution of the 5 μm linewidth via chains from 32 nm wafers as a function of temperature in the range of 125 ºC to 275 ºC. No SM fails were measured from the 325 ºC test.

Equation (1) was used to fit the five-temperature failure distributions from the PL-SM data of the 5 μm via chains as shown in [2,3]. During the fitting process, parameters of T_0 , N and E_A are allowed to vary to minimize the standard fitting error function. As results, the T_0 value is 277 ºC, N is 1.25, and E_A is 0.72 eV in this case. The results of fitting parameters were applied to (1) and the calculated MTF values are shown as model fit in Figure 3. The model fit calculations and the MTF SM data distributions are consistent with each other. It is necessary to point out that the E_A value can vary depending on the quality of Cu/cap interface and Cu grain boundary diffusion. A relative weak Cu/cap interface assisted by gain boundary diffusion will lower the E_A. The E_A values can be in the range of ~1.0 eV to 0.5 eV.

2.2 Stress temperature (cont'd)

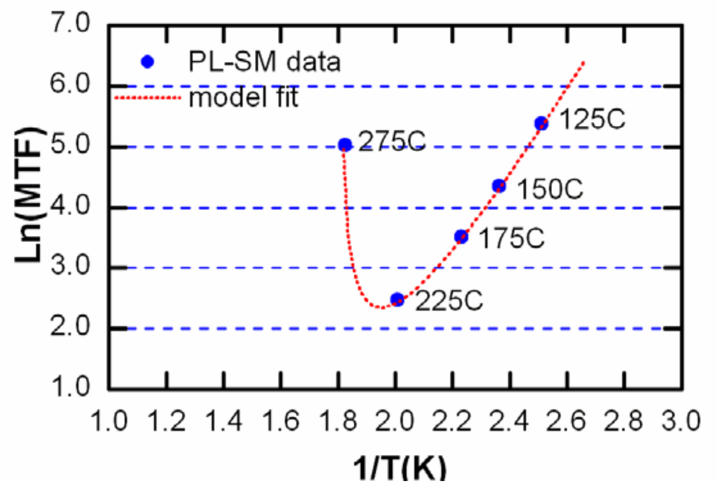

Figure 1 — Temperature dependent behavior of SM MTF values of 5 µm via chains in the range of 125 °C - 275 °C

The results shown in Figure 1 demonstrate the following important SM behavior: 1) above T_0, no SM fails will occur due to the compressive thermo-mechanical stress. The fact we have measured no SM fails from the 325 °C tests confirms this; 2) MTF increases as temperature decreases below T_0. MTF reaches its minimum at a "sweet spot" near 200 °C to 225 °C. The location of the "sweet spot" may vary depending on wafer process details; 3) below T_0 but above the "sweet spot", the MTF distribution reverses its direction; 4) Close to the operating temperature range, i.e., ~125 °C to 100 °C, the SM data are mostly Arrhenius-like and dominated by the diffusion term. The temperature dependence below the "sweet spot" (i.e., ~175 °C to 100 °C) can be approximately treated by Arrhenius model.

2.3 Geometry linewidth dependence of SIV risk

The linewidth dependence of SIV risk is an important feature for setting design rules and reliability qualification tests. As we have shown in section A that SM MTF values are linewidth dependent. In general, the SIV risk increases as linewidth increases for a single via. The MTF values follow a power-law as a function of linewidth as shown in Figure 2. The MTF power-law relation can be expressed as:

$$MTF=CW^{-2.94} \qquad (2)$$

where W is the linewidth or plate size and C is a normalization constant. 2.94 is the power-law component value from the fit.