JEDEC STANDARD

POD125 - 1.25 V Pseudo Open Drain I/O

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POD125 - 1.25 V PSEUDO OPEN DRAIN I/O

(From JEDEC Board Ballot JCB-17-25, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the DC and AC single-ended (data) and differential (clock) operating conditions, I/O impedances, and the termination and calibration scheme for 1.25 V Pseudo Open Drain I/Os.

The 1.25 V Pseudo Open Drain interface, also known as POD125, is primarily used to communicate with GDDR6 SGRAM devices.

Multiple Classes of POD125 are expected to reside within the family of POD125 interfaces in order to accommodate various device and market applications. The various classes standardized within the context of POD125 are documented in the appendices of this document (e.g., POD125/Class A).

The core of this standard documents the subset of values common to all Classes of POD125 and documents specification items left to definition within a specific Class as denoted by CDV which is defined as Class Dependent Value.

The values specific to each particular class of POD125 are found in the annexes. See specific Class tables for further details.

NOTE It does not follow that all specification values defined in a given Class are necessarily different from the matching parameter in other Class within POD125. Multiple Classes may reuse a given specification value if appropriate to the Class requirements.

2 Core POD125 Interface Standard

Table 1 — DC Operating Conditions

Parameter	Symbol	POD125			Unit	Notes
		Min	Typ	Max		
Device Supply Voltage	V_{DD}	1.2125	1.25	1.2875	V	1
Output Supply Voltage	V_{DDQ}	1.2125	1.25	1.2875	V	1
Reference voltage: DQ and DBI_n pins	V_{REFD}	CDV		CDV	V	3, 4
	V_{REFD2}	CDV		CDV	V	3, 4, 5
Reference voltage: CA pins	V_{REFC}	CDV		CDV	V	6
	V_{REFC2}	CDV		CDV	V	6, 7
DC input logic HIGH voltage with V_{REFC}: CA	V_{IHA}(DC)	CDV			V	8
DC input logic LOW voltage with V_{REFC}: CA	V_{ILA}(DC)			CDV	V	8
DC input logic HIGH voltage with V_{REFC2}: CA	V_{IHA2}(DC)	CDV			V	8
DC input logic LOW voltage with V_{REFC2}: CA	V_{ILA2}(DC)			CDV	V	8
DC input logic HIGH voltage with V_{REFD}: DQ, DBI_n	V_{IHD}(DC)	CDV			V	8
DC input logic LOW voltage with V_{REFD}: DQ, DBI_n	V_{ILD}(DC)			CDV	V	8
DC input logic HIGH voltage with V_{REFD2}: DQ, DBI_n	V_{IHD2}(DC)	CDV			V	8
DC input logic LOW voltage with V_{REFD2}: DQ, DBI_n	V_{ILD2}(DC)			CDV	V	8
RESET_n and boundary scan input logic HIGH voltage; EDC and CA input logic high voltage for x16/x8 mode, PC vs. 2-channel mode, CK and CA ODT select at reset	V_{IHR}	CDV			V	8
RESET_n and boundary scan input logic LOW voltage; EDC and CA input logic low voltage for x16/x8 mode, PC vs. 2-channel mode, CK and CA ODT select at reset	V_{ILR}			CDV	V	8
Input leakage current (any input 0V <= V_{IN} <= V_{DDQ}; all other signals not under test = 0V)	I_L				µA	
Output leakage current (outputs are disabled; 0V <= V_{OUT} <= V_{DDQ})	I_{OZ}				µA	
Output logic LOW voltage	VOL(DC)			0.52	V	
Single ended clock input voltage level: CK_t, CK_c, WCK_t, WCK_c	V_{IN}	-0.30		V_{DDQ} + 0.30		13
Clock input mid-point voltage: CK_t, CK_c	V_{MP}(DC)	V_{REFC} - 0.10		V_{REFC} + 0.10	V	9, 12
Clock input differential voltage: CK_t, CK_c	V_{IDCK}(DC)	CDV			V	10, 12
Clock input differential voltage: WCK_t, WCK_c	V_{IDWCK}(DC)	CDV			V	11, 14

NOTE 1 GDDR6 SGRAMs are designed to tolerate PCB designs with separate V_{DD} and V_{DDQ} power regulators.
NOTE 2 DC bandwidth is limited to 20 MHz.
NOTE 3 AC noise in the system is estimated at 50mV pk-pk for the purpose of DRAM design.
NOTE 4 The reference voltage source and control for DQ and DBI_n pins are determined by Half V_{REFD} and V_{REFD} Level mode register bits.
NOTE 5 Programmable V_{REFD} levels are not supported with V_{REFD2}.
NOTE 6 The reference voltage source (external or internal) is determined at power-up; the reference voltage level is determined by Half V_{REFC} and the V_{REFC} Offset mode register bits.
NOTE 7 Programmable V_{REFC} offsets are not supported with V_{REFC2}.
NOTE 8 V_{IHR} and V_{ILR} apply to boundary scan input pins TDI, TMS and TCK. V_{IHR} and V_{ILR} apply to EDC and CA inputs at reset when latching default device configurations. V_{IHR} and V_{ILR} also apply to CA, CABI_n, CKE_n, CK, DQ, DBI_n, EDC and WCK inputs when boundary scan mode is active and input data are latched in the Capture-DR TAP controller state.
NOTE 9 This provides a minimum of 0.775 V to a maximum of 0.975 V, and is normally 70% of V_{DDQ}. DRAM timings relative to CK_t cannot be guaranteed if these limits are exceeded.
NOTE 10 V_{IDCK} is the magnitude of the difference between the input level in CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is V_{REFC}.
NOTE 11 V_{IDWCK} is the magnitude of the difference between the input level in WCK_t and the input level on WCK_c. The input reference level for signals other than WCK_t and WCK_c is either V_{REFC}, V_{REFC2}, V_{REFD} or V_{REFD2}.
NOTE 12 The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross. Please refer to the applicable timings in the AC Timings table.
NOTE 13 Use V_{IHR} and V_{ILR} when boundary scan mode is active and input data are latched in the Capture-DR TAP controller state.
NOTE 14 The WCK_t and WCK_c input reference level (for timing referenced to WCK_t and WCK_c) is the point at which WCK_t and WCK_c cross. Please refer to the applicable timings in the AC Timings table.