JEDEC STANDARD

Stress-Test-Driven Qualification of Integrated Circuits

JESD47J.01

(Revision of JESD47J, August 2017)

SEPTEMBER 2017

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2017
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

PRICE: Contact JEDEC

STRESS DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS

(From JEDEC Board Ballot, JCB-17-09, formulated under the cognizance of the JC14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

This standard describes a baseline set of acceptance tests for use in qualifying electronic components as new products, a product family, or as products in a process which is being changed.

These tests are capable of stimulating and precipitating semiconductor device and packaging failures. The objective is to precipitate failures in an accelerated manner compared to use conditions. Failure Rate projections usually require larger sample sizes than are called out in qualification testing. For guidance on projecting failure rates, refer to JESD85 Methods for Calculating Failure Rates in Units of FITs. This qualification standard is aimed at a generic qualification for a range of use conditions, but is not applicable at extreme use conditions such as military applications, automotive under-the-hood applications, or uncontrolled avionics environments, nor does it address 2nd level reliability considerations, which are addressed in JEP150. Where specific use conditions are established, qualification testing tailored to meet those specific requirements can be developed, using JESD94 that will result in a better optimization of resources.

This set of tests should not be used indiscriminately. Each qualification project should be examined for:
a) Any potential new and unique failure mechanisms.
b) Any situations where these tests/conditions may induce invalid or overstress failures.

If it is known or suspected that failures either are due to new mechanisms or are uniquely induced by the severity of the test conditions, then the application of the test condition as stated is not recommended. Alternatively, new mechanisms or uniquely problematic stress levels should be addressed by building an understanding of the mechanism and its behavior with respect to accelerated stress conditions (Ref. JESD91, “Method for Developing Acceleration Models for Electronic Component Failure Mechanisms” and JESD94, “Application Specific Qualification using Knowledge Based Test Methodology”).

Consideration of PC board assembly-level effects may also be necessary. For guidance on this, refer to JEP150, Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components.

This document does not relieve the supplier of the responsibility to assure that a product meets the complete set of its requirements.

2 Reference documents

The revision of the referenced documents shall be that which is in effect on the date of the qualification plan.

2.1 Military

MIL-STD-883, *Test Methods and Procedures for Microelectronics*

MIL-PRF 38535

2.2 Industrial

UL94, *Tests for Flammability of Plastic Materials for Parts in Devices and Appliances.*

ASTM D2863, *Flammability of Plastic Using the Oxygen Index Method.*

IEC Publication 695, *Fire Hazard Testing.*

J-STD-020, Joint IPC/JEDEC Standard, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface-Mount Devices*.

JP-001, *Foundry Process Qualification Guidelines (Wafer Fabrication Manufacturing Sites).*

JS-001, *Joint JEDEC/ESDA Standard for Electrical Discharge Sensitivity Test - Human Body Model (HBM) – Component Level*

JS-002, *ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level*

J-STD-002, *Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires*

JESD22 Series, *Reliability Test Methods for Packaged Devices*

JESD46, *Guidelines for User Notification of Product/process Changes by Semiconductor Suppliers.*

JESD69, *Information Requirements for the Qualification of Silicon Devices*.

JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components*.

JESD78, *IC Latch-Up Test*.

JESD85, *Methods for Calculating Failure Rates in Units of FITs*.

JESD86, *Electrical Parameters Assessment*.

JESD94, *Application Specific Qualification using Knowledge Based Test Methodology.*

JESD91, *Methods for Developing Acceleration Models for Electronic Component Failure Mechanisms*.

JEP122, *Failure Mechanisms and Models for Semiconductor Devices*.

JEP143, *Solid State Reliability Assessment Qualification Methodologies.*

JEP150, *Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components.*

JESD201, *Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes*

3 General requirements

3.1 Objective

The objective of this procedure is to ensure that the device to be qualified meets a generally accepted set of stress test driven qualification requirements. Qualification is aimed at components used in commercial or industrial operating environments.

3.2 Qualification family

While this specification may be used to qualify an individual component, it is designed to also qualify a family of similar components utilizing the same fabrication process, design rules, and similar circuits. The family qualification may also be applied to a package family where the construction is the same and only the size and number of leads differs. Interactive effects of the silicon and package shall be considered in applying family designations.

3.3 Lot requirements

Test samples shall comprise representative samples from the qualification family. Manufacturing variability and its impact on reliability shall be assessed. Where applicable the test samples will be composed of approximately equal numbers from at least three (3) nonconsecutive lots. Other appropriate means may be used to evaluate manufacturing variability. Sample size and pass/fail requirements are listed in Tables 1-3. Tables A and B give guidance on translating pass/fail requirements to larger sample sizes.

Generic data and larger sample sizes may be employed based upon a Chi Squared distribution using a total percent defective at a 90% confidence limit for the total required lot and sample size. ELFR requirements shall be assessed at a 60% confidence level as shown in Table B. If a single unique and expensive component is to be qualified, a reduced sample size qualification may be performed using 1/3 the sample size listed in the qualification tables.

3.4 Production requirements

All test samples shall be fabricated and assembled in the same production site and with the same production process for which the device and qualification family will be manufactured in production. Samples need to be processed through the full production process including burn-in, handling, test, and screening.

3.5 Reusability of test samples

Devices that have been used for nondestructive qualification tests may be used to populate other qualification tests. Devices that have been used in destructive qualification tests may not be used in subsequent qualification stresses except for engineering analysis. Non-destructive qualification tests are: Early Life Failure Rate, Electrical Parameters Assessment, External Visual, System Soft Error, and Physical Dimensions.