

IPC-7091

2017 - June

**Design and Assembly Process
Implementation of 3D Components**

An international standard developed by IPC

Association Connecting Electronics Industries



The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee (TAEC) adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

Notice

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

IPC Position Statement on Specification Revision Change

It is the position of IPC's Technical Activities Executive Committee that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC publication is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision. Adopted October 6, 1998

Why is there a charge for this document?

Your purchase of this document contributes to the ongoing development of new and updated industry standards and publications. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards and publications development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low to allow as many companies as possible to participate. Therefore, the standards and publications revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards and publications, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit www.ipc.org or call 847/597-2872.

Thank you for your continued support.



IPC-7091

Design and Assembly Process Implementation of 3D Components

Developed by the 3-D Electronic Packages Subcommittee (B-11) of the
Packaged Electronic Components Committee (B-10) of IPC

Users of this publication are encouraged to participate in the
development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 105N
Bannockburn, Illinois
60015-1249
Tel 847 615.7100
Fax 847 615.7105

This Page Intentionally Left Blank

Acknowledgment

Any document involving a complex technology draws material from a vast number of sources across many continents. Shown below are the principal members of the 3-D Electronic Packages Subcommittee (B-11) of the Packages Electronic Components Committee (B-10). It is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

Packaged Electronic Components Committee	Electronic Packages Subcommittee	Technical Liaison of the IPC Board of Directors
Chair Vern Solberg Solberg Technical Consulting	Co-Chair Dudi Amir Intel Corporation	Bob Neves Microtek Laboratories
Vice Chair Russell H. Nowland Nokia	Co-Chair Vern Solberg Solberg Technical Consulting	
Electronic Packages Subcommittee		
Richard A. Allen, National Institute of Standards & Technology	Maurice LeBlon, AI Technologies, Inc.	Jagadeesh Radhakrishnan, Intel Corporation
Dudi Amir, Intel Corporation	Steven Martell, Sonoscan Inc.	Herb Reiter, Eda2asic Consulting
Kjell Asp, Saab Bofors Dynamics AB	Richard McKee, PacTech USA Packaging Technologies Inc.	Witold Roman, Wabtec Railway Electronics
Stephen V.Chavez, UTC Aerospace Systems	Craig Mitchell, Tessera Technologies, Inc.	Jeff Shubrooks, Raytheon Company
Marie Cole, IBM Corporation	Alton Moore, Raytheon Company	Vanessa Smet, Georgia Institute of Technology
Michael Durkan, Mentor Graphics Corporation	Michael Moore, U.S. Army Aviation & Missile Command	Vern Solberg, Solberg Technical Consulting
Dennis Fritz, MacDermid Enthone Electronics Solutions	Richard Otte, PROMEX Industries, Inc.	Bhanu Sood, NASA Goddard Space Flight Center
Ife Hsu, Intel Corporation	Joel S. Peiffer, 3M Company	Mamoru Takahashi, Asahi Glass Co., Ltd.
Jay Huang, Teledyne Dalsa	Keith A. Peterson, Missile Defense Agency	Marc Theeuwes, Jabil
Bruce V. Hughes, AMRDEC MS&T EPPT	Ray Prasad, Ray Prasad Consultancy Group	Steve J. Vetter, NSWC Crane
Jennie S.Hwang, H-Technologies Group	Raj Pulugurtha, Georgia Institute of Technology	Charles Woychik, Invensas Corporation
Rajesh C.Kumar, TTM Technologies		

Special Recognition

In addition to the individuals recognized for their contributions, IPC thanks PROMEX Industries, Inc., Santa Clara, CA; Intel Corporation, Hillsboro, OR; and Axiom Electronics, Beaverton, OR, for hosting B-11 Subcommittee working meetings to develop IPC-7091.

This Page Intentionally Left Blank

Table of Contents

1	SCOPE	1	4.2.1	Cleaning	10
1.1	Purpose	1	4.2.2	Baking	11
1.2	Target Audience	1	4.2.3	Changing Termination Material	11
1.3	Intent	1	4.3	Passive-Component Integration (Organic Base Material)	12
1.4	Definition of Requirements	1	4.3.1	Formed Resistors	13
1.5	Implementation Challenges	1	4.3.2	Formed Capacitors	13
2	APPLICABLE DOCUMENTS	3	4.3.3	Formed Inductors	13
2.1	IPC	3	4.3.4	Discrete Inductors	13
2.2	Joint Industry Standards	3	4.4	Passive Component Integration (Nonorganic Base Material)	14
2.3	JEDEC	4	4.4.1	Formed Resistors	14
2.4	Government Electronics and Information Technology Association (GEIA)	4	4.4.2	Formed Capacitors	14
3	GENERAL DESCRIPTION	4	4.4.3	Formed Inductors	15
3.1	Terms and Definitions	4	4.5	Semiconductor Die Issues	15
3.1.1	Die*	4	4.5.1	Surface Redistribution	15
3.1.2	Electronic Element	4	4.6	Postprocess Validations	16
3.1.3	Interposer	5	4.6.1	Solder on Pad (Flip-Chip)	16
3.1.4	Substrate	5	4.6.2	Known Good Die (KGD)	16
3.1.5	Electronic Package	5	4.7	Package Assembly Variations	16
3.1.6	Electronic Module	5	4.7.1	Die Stack (Wire Bond)	16
3.1.7	Three-Dimensional (3D) Packaging	5	4.7.2	Package-on-Package (PoP) Technologies	17
3.2	Technology Overview	5	4.7.3	Through Mold Via (TMV)	18
3.2.1	Die Stack Package	5	4.7.4	Through-Mold Interconnect (TMI)	18
3.2.2	Package Stack	5	4.7.5	High-Density Package-on-Package (PoP)	19
3.2.3	Package-on-Package (PoP)	5	4.7.6	Folded Stack Packaging	20
3.2.4	Interposer	6	4.7.7	Package-on-Package Interposer (PoPi)	21
3.2.5	Through-Silicon Via (TSV)	6	4.7.8	Thin Small Outline Package (TSOP) Stacking	21
3.2.6	Through-Glass Via (TGV)	6	4.7.9	Die Stack Copper-to-Copper Through- Silicon Via (TSV)	21
3.2.7	System on Chip (SoC)	6	4.7.10	Three-Dimensional (3D) Interposer/ Substrate Packaging	23
3.2.8	System in Package (SiP)	6	4.8	Cost Consideration	23
3.2.9	Wafer-Level Packaging (WLP)	7	4.9	Component Handling	23
3.2.10	Fan-Out Wafer-Level Packaging (FOWLP)	7	4.9.1	Packaging	23
3.2.11	Substrate	7	4.9.2	Component Storage	24
3.3	Package Geometric Space	7	4.10	Thermal Management of 3D Components	24
3.3.1	Two-Dimensional (2D) Package	7	4.10.1	Thermal Conduction/Convection	24
3.3.2	Two-and-a-Half-Dimensional (2.5D) Package	8	4.10.2	Thermal Transfer Mechanisms	25
3.3.3	Three-Dimensional (3D) Package	8	4.10.3	Advanced Thermal Interface Materials	26
3.4	Embedded (Placed) Technology	9	4.10.4	High-Conductivity Mold Compounds	27
4	DEVICE CONSIDERATIONS	10	4.10.5	Liquid Cooling	28
4.1	General Requirements	10	4.10.6	Microfluidic Cooling	28
4.2	Device Preparation	10			

4.10.7	Single-Phase Intertier Cooling	28	8.3.7	Immersion Tin	41
4.10.8	Two-Phase Intertier Cooling	28	8.3.8	Copper (Chemical Deposition and Electroplate)	41
4.10.9	Heat Pipes	29	8.4	Embedded-Component Technology	41
4.10.10	Microchannel and Minichannel Cooling	29	8.4.1	Formed Resistor Process	41
4.10.11	Thermal Modeling	29	8.4.2	Capacitor Formation Process	43
5	INTERPOSER/SUBSTRATE MATERIALS	30	8.4.3	Planar Capacitance	43
5.1	Organic Interposer	30	8.4.4	Discrete Formed Capacitor Element	43
5.2	Glass Interposer	30	8.4.5	Discrete Inductor Forming	43
5.3	Silicon Interposers	31	8.4.6	Discrete Component Placement	43
5.4	Ceramic Substrate/Interposer	31	8.5	Substrate and Interposer Materials (Package Level)	45
5.5	Conductor Characteristics (Copper Foil/Film)	31	8.5.1	Organic Circuit Structure	46
5.6	Conductor Characteristics (Metallization on Silicon)	32	8.5.2	Ceramic Circuit Structure	46
5.7	Conductor Characteristics (Metallization on Glass)	32	8.5.3	Silicon Circuit Structure	46
5.8	Conductor Characteristics (Metallization on Ceramic)	32	8.5.4	Glass Circuit Structure	46
6	PROCESS MATERIALS	33	8.6	Dielectric Encapsulation	46
6.1	Adhesives (Conductive and Nonconductive)	33	8.6.1	Reinforced Prepreg	46
6.1.1	Polymer Adhesives	33	8.6.2	Unreinforced Resin	47
6.1.2	Dry-Film Adhesive	34	8.6.3	Resin-Coated Copper (RCC)	47
6.2	Solder Materials	34	8.7	Via Hole Preparation and Interconnectivity	47
7	PACKAGE-LEVEL STANDARDIZATION	35	8.7.1	Through-Glass Via (TGV) Connection to PWB Copper	47
7.1	Package Outline Standards	35	8.7.2	Through-Glass Via (TGV) Connection to Component Terminations	47
7.1.1	Ball Grid Array (BGA)	36	8.7.3	Through-Glass Via (TGV) Formation	47
7.1.2	Fine-Pitch BGA (FBGA/FIBGA)	36	8.7.4	Through-Silicon Via (TSV) Formation	48
7.1.3	Package-on-Package (PoP)	37	8.7.5	Via Filling	48
7.1.4	Through-Mold Via (TMV) Package-on-Package (PoP)	38	8.7.6	Alternative Via Plating on Silicon-Based Interposers	48
7.1.5	Wafer-Level Ball Grid Array (WLBGA)	38	8.7.7	Conductor Forming on Silicon Interposers	49
7.1.6	Stacked-Die Packaging Standards	39	8.8	Build-Up Layers and Via Hole Preparation – Redistribution Layer (RDL) on Silicon and Glass	49
8	PWB AND OTHER MOUNTING BASE OR PWB STACK-UP CONSIDERATIONS	39	8.8.1	Silicon Interposer Metallization	49
8.1	PWB Technology	39	8.8.2	Glass Interposer Metallization	49
8.1.1	Multilevel Substrate	40	9	DESIGN METHODOLOGY	49
8.2	Mounting Base	40	9.1	Design Challenges	49
8.3	Surface Finish for Placed Components	40	9.2	Total Circuit Consideration	49
8.3.1	Electroless Nickel/Immersion Gold (ENIG)	40	9.2.1	Internal (Embedded) Component Mounting	50
8.3.2	Electroless Nickel/Electroless Palladium/ Immersion Gold (ENEPIG)	40	9.2.2	External (Surface) Component Mounting	50
8.3.3	Organic Solderability Preservative (OSP)	40	9.2.3	Internal (Embedded) Component Mounting	51
8.3.4	Electrolytic Nickel/Electrolytic Gold (ENEG)	41	9.2.4	Circuit Interface Techniques	51
8.3.5	Direct Immersion Gold (DIG)	41	9.2.5	Internal Discrete Heat Sink	51
8.3.6	Immersion Silver	41	9.3	Layout Strategy	51
			9.3.1	Product Functional Description	53
			9.3.2	Engineering Actions	53

9.3.3	Design Density Analysis	53	10.6	Three-Dimensional (3D) Component Inspection Techniques	64
9.3.4	Embedded Component Selection	53	10.7	Board-Level Rework	65
9.3.5	Embedded-Component Circuit Interface	54	10.7.1	Rework With Convection Reflow Soldering ...	66
9.4	Multilayer Substrate Construction and Geometries	55	10.7.2	Rework With Infrared (IR) Reflow Soldering	66
9.4.1	Build-Up Circuit Layers on Glass Base Structures	55	10.7.3	Rework With Laser Soldering	66
9.4.2	Build-Up Circuit Layers on Silicon Base Structures	55	10.8	Underfill	66
9.5	Component Attachment on Multilevel Assembly	55	10.8.1	Package-to-PWB Reinforcement	66
9.5.1	Conductive Polymers	55	10.9	Material Selection and Application	67
9.5.2	Dry-Film Adhesives	55	10.9.1	Capillary Flow Underfill	67
9.5.3	Solder Attachment	56	10.9.2	No-Flow/Fluxing Underfill	67
9.6	Circuit Routing Strategy (Organic and Nonorganic)	56	10.9.3	Removable and Reworkable Underfill	68
9.6.1	Organic-Based Substrates	56	10.9.4	Corner Bonding/Glue Bonding	68
9.6.2	Silicon and Glass Interposers	56	10.9.5	Molded Underfill	68
9.6.3	Ceramic-Based Substrates and Interposers	56	10.9.6	Vacuum Underfill (VUF)	68
9.7	Documentation	56	10.9.7	Wafer-Applied Underfill	68
9.7.1	Documentation Package	56	10.9.8	Underfill Inspection	69
9.7.2	Bill of Materials (BoM)	57	11	TESTING AND PRODUCT VERIFICATION	70
9.7.3	Software Tools and Data Transfer	57	11.1	Establishing Test Requirements	70
9.7.4	General Rules for 3D Design	57	11.2	Assembly Process Qualification	70
10	ASSEMBLY OF 3D PACKAGES ON PWBs	57	11.2.1	Package-Level Stress Test	70
10.1	Package-on-Package (PoP) Assembly Process	57	11.3	Substrate Test Coupons	71
10.1.1	Package-on-Package (PoP) Fluxing Options ...	58	12	RELIABILITY	72
10.1.2	Package-on-Package (PoP) Fluxing Process ...	58	12.1	Reliability Considerations	72
10.1.3	Flux Height Statistical Process Control	59	12.2	Design for Reliability (DfR) Principles	73
10.1.4	Paste Dip	60	12.3	End-Use Relationship	73
10.1.5	Prestacking Process	60	12.4	Effects of Pb-Free Materials and Pure-Tin Finishes on Reliability	73
10.1.6	Through-Mold Via (TMV)/Through-Mold Interconnect (TMI) Assembly Considerations	60	12.5	Validation, Qualification and Accelerated Aging Test for Reliability	73
10.1.7	Package-on-Package (PoP) Stand-Off Height (SOH)	61	12.6	Environmental Testing	75
10.1.8	Package-on-Package (PoP) Die Gap	62	13	DEFECT AND FAILURE ANALYSIS	76
10.2	Three-Dimensional (3D) Printing	62	13.1	Nondestructive Failure Analysis	76
10.2.1	Jet Printing	62	13.1.1	Electrical Testing	77
10.2.2	Cavity Printing	62	13.2	Internal Nondestructive Inspection	77
10.2.3	Cavity Keep-Out Zone	63	13.2.1	Acoustic Microscopy (AM)	77
10.3	Multilevel Placement	63	13.2.2	X-Ray Imaging	77
10.4	Die Attachment	63	13.2.3	Infrared (IR)	78
10.4.1	Direct Chip Attachment	63	13.2.4	Magnetic Current Imaging (MCI)	78
10.4.2	Die-to-Substrate Reinforcement	63	13.2.5	Internal Optical Inspection	78
10.5	Reflow Soldering Considerations for 3D Components	64	13.2.6	Electrical Probing/Nanoprobing	78
			13.2.7	Chemical Analysis	79
			13.3	Destructive Failure Analysis	79
			13.3.1	Cross-Sectioning	79
			13.3.2	Parallel Lapping	80

13.3.3	Decapsulation	80	Figure 4-12	Lower Package-on-Package (PoP) Section With Through Mold Interconnect (TMI)	19
13.4	Optical Inspection	81	Figure 4-13	Copper Pillar Interconnect (CuPI) Package-on-Package (PoP)	19
13.4.1	Optical Inspection (After Assembly)	81	Figure 4-14	High-Density Micro-Pillar (μ PILR) Array Packaging	19
13.4.2	Confocal Laser Scanning Microscopy (CLSM)	81	Figure 4-15	Bond Via Array (BVA) With Fine-Pitch Copper Wire Interconnect	20
13.4.3	Examples of Observed External Inspection Defects	81	Figure 4-16	Direct Bond Interface (DBI)	20
14	SUPPLIER SELECTION AND QUALIFICATION	83	Figure 4-17	Three-Memory Die on Flexible Circuit Substrate	20
14.1	Factory and Process Audits	83	Figure 4-18	Package-on-Package Interposer (PoPi)	21
14.2	Site Visit Procedure	83	Figure 4-19	Stacked Thin Small Outline Package (TSOP) Devices	21
14.3	Design and Process Evaluation	83	Figure 4-20	Fusion Bond Process	22
14.4	Observations and Recommendations	84	Figure 4-21	Intermetallic Bonds (Cu/Cu ₃ Sn/Cu)	22
15	GLOSSARY OF ACRONYMS	85	Figure 4-22	Partitioned Carrier Trays for Ball Grid Array (BGA) Components	23
Figures					
Figure 1-1	3D Technology Complexity	2	Figure 4-23	Thermal Conduction	24
Figure 3-1	Die Stack Package Assembly	5	Figure 4-24	Thermal Transfer Paths	25
Figure 3-2	Mixed-Function Package-on-Package (PoP) Example	6	Figure 4-25	Thermal Resistance Versus Bondline Thickness for State-of-the-Art Thermal Greases and Gels	26
Figure 3-3	System on Chip (SoC) Example	6	Figure 4-26	Advances in Thermal Resistance With Thinner and Higher-Conductivity Reliable Materials	26
Figure 3-4	System in Package (SiP) Example	7	Figure 4-27	Nanosilver Interconnections	27
Figure 3-5	Wafer-Level Packaging (WLP) for High-Performance Memory	7	Figure 4-28	Advances in 3D Packages With Fan-Out Wafer-Level Packaging (FOWLP) and Die-Embedding (Left) and High-Thermal-Conductivity Composites With Advanced Boron Nitride Fillers and Surface Treatments (Right)	27
Figure 3-6	Example of a 2D System in Package	8	Figure 4-29	Liquid Heat Pipe Exchange System	28
Figure 3-7	Example of a 2.5D System in Package (SiP)	8	Figure 4-30	Comparison of 3D Integrated Circuits (ICs) Utilizing Different Cooling Technologies	29
Figure 3-8	3D Package-on-Package (PoP) and System in Package (SiP) on a PWB	9	Figure 5-1	Simulated Insertion Loss (S_{21}) of Through-Glass Via (TGV) and Through-Silicon Via (TSV) Interconnects	30
Figure 3-9	Ball Grid Array (BGA) Substrate With Embedded Active and Passive Elements	9	Figure 5-2	Glass Wafer and Panel Substrates	30
Figure 4-1	Benchtop Small-Batch Ultrasonic Cleaner	10	Figure 5-3	Microcrystalline-Silicon Ingot	31
Figure 4-2	JEDEC-Compliant Carrier Tray	11	Figure 5-4	Flattened Feature on Wafer Edge Identifies Wafer Orientation During Fabrication Processes	31
Figure 4-3	SnPb and Mixed-Metallurgy Ball Grid Array (BGA) Solder Joints	12	Figure 5-5	Ceramic Panel Prior to Metallization	31
Figure 4-4	Formed Resistor Elements	13	Figure 7-1	Ball Grid Array (BGA) Package Outline	36
Figure 4-5	Trench or Pillar Capacitor in Silicon	14	Figure 7-2	Fine-Pitch Ball Grid Array (FBGA/FIBGA)	36
Figure 4-6	Surface Redistribution	15	Figure 7-3	Fine-Pitch Ball Grid Array (FBGA/FIBGA) Contact Diameter and Pitch Variations	37
Figure 4-7	Contact Variations for Flip-Chip Mounting	16			
Figure 4-8	Comparing Current Two-Die and Quad-Die Package Solutions	17			
Figure 4-9	Through-Mold Via (TMV) Package-on-Package (PoP)	17			
Figure 4-10	Through-Mold Via (TMV) Solder Balls	18			
Figure 4-11	Lower Package-on-Package (PoP) Section With Through-Mold Vias (TMVs)	18			

Figure 7-4	JEDEC Package-on-Package (PoP) Construction Variations	38	Figure 10-10	Z-Height of a Package-on-Package (PoP) ...	61
Figure 7-5	Contact Redistribution at the Wafer Level Provides a Method for Furnishing a Uniform Array Format to Better Accommodate Face-Down Mounting	38	Figure 10-11	Joint Stand-Off Height (SOH)	61
Figure 8-1	Two-Level Substrate With Embedded Components	40	Figure 10-12	Package-on-Package (PoP) Die Gap	62
Figure 8-2	Ball Grid Array (BGA) Package Adopting an Embedded-Component Substrate	41	Figure 10-13	Cavity and 3D Stencil	62
Figure 8-3	Pull-Up and Pull-Down Resistors Using Thin-Film Material	42	Figure 10-14	Three-Dimensional (3D) Stencil With a Cavity Pocket on the Right	62
Figure 8-4	Formed Multilayer Capacitor Element	43	Figure 10-15	Slit-Metal Squeegee	62
Figure 8-5	Etched Copper Spiral Inductor Pattern	43	Figure 10-16	Package-on-Package (PoP) Mounted Into a Cavity	63
Figure 8-6	0201 Components Embedded Into a Cavity Feature in the Substrate	44	Figure 10-17	Cavity Keep-Out Zone	63
Figure 8-7	Three-Dimensional (3D) Die Stack Package Using Copper Wire-Bond Processing	45	Figure 10-18	Multilevel PWB	63
Figure 8-8	Additive Redistribution Layer (RDL) to Array Contact Site	45	Figure 10-19	Capillary Flow of Liquid Epoxy Fully Encapsulating and Stabilizing the Area Between Two Parallel Surfaces	64
Figure 8-9	Merging Organic and Silicon-Based Materials for 3D Semiconductor Packaging	45	Figure 10-20	Soldering Material in Package-on-Package (PoP) Assembly	64
Figure 8-10	Ceramic-Based Interposer	46	Figure 10-21	Package-on-Package (PoP) With Overlapping Memory Balls	64
Figure 8-11	Through-Glass Via (TGV)	47	Figure 10-22	Package-on-Package (PoP) With Overlapping Memory Balls Viewed With Laminography X-Ray	65
Figure 8-12	Through-Glass Via (TGV)-Formed Glass Substrates	47	Figure 10-23	Head on Pillow (HoP) 3D Image	65
Figure 8-13	Metallized Through-Glass Via (TGV) X-Ray Photos	48	Figure 10-24	2D X-Ray View of Through-Mold Interconnect (TMI) Package-on-Package (PoP) With Head on Pillow (HoP) Defect on the Memory	66
Figure 8-14	Copper-Filled Through-Silicon Via (TSV) Interface Between Wafers – Active Side and Back Side	48	Figure 10-25	Package-to-PWB Reinforcement	67
Figure 8-15	Comparing Via Deposition Methodology	49	Figure 10-26	Edge Dispensing of Underfill Material	67
Figure 9-1	Embedded Semiconductor Substrate	54	Figure 10-27	Comparing Two-Step Underfill Plus Mold Process (A) to the One-Step Molded Underfill Packaged Die (B)	68
Figure 9-2	Glass Interposer With 40- μm Pitch Bumps and L/S = 2 μm / 2 μm	55	Figure 10-28	Void in Underfill Under Array-Configured Flip-Chip Die	69
Figure 9-3	Two-Layer Build-Up Circuit Interposer	55	Figure 11-1	Quality Document System	71
Figure 10-1	Package-on-Package (PoP) Assembly Principle	58	Figure 13-1	Acoustical Microscopy (AM) Can Identify Voids, Delamination and Cracks	77
Figure 10-2	Package-on-Package (PoP) Fluxing Units	58	Figure 13-2	3D Submicron X-Ray Imaging Distinctly Identifying Solder Bridging	77
Figure 10-3	Ball Grid Array (BGA) Flux Coverage	59	Figure 13-3	Die-to-Silicon-to-Substrate Assembly	79
Figure 10-4	Flux Transfer to a Copper Coupon	59	Figure 13-4	Semiconductor Package Decapsulation System	80
Figure 10-5	Flux Height Measurement Gauges	60	Figure 13-5	Head on Pillow (HoP) Solder Process Defect	81
Figure 10-6	Solder Balls After Paste Dip	60	Figure 13-6	Poor Coalesce Between Sphere and Interposer Land	81
Figure 10-7	Carrier With Prestacked Packages	60	Figure 13-7	Nonwetting Defect, Exhibiting the Effect of Excessive Oxidation	81
Figure 10-8	Soldering Surface of Through-Mold Via (TMV) Balls	60			
Figure 10-9	Ball Collapse	61			

Figure 13-8	Endoscopy Edge View of Solder Bridge Between Ball Grid Array (BGA) Sphere Contacts	81
Figure 13-9	Defect Attributed to Oxide Contamination	82
Figure 13-10	Comparison of Wetting Characteristics of Two Surface Finishes	82

Tables

Table 4-1	Through-Mold Via (TMV) Examples	18
Table 6-1	Common Pb-Free Solder Paste Compositions	35
Table 7-1	Plastic Ball Grid Array (PBGA) Contact Diameter and Pitch Variations	36
Table 7-2	Fine-Pitch Ball Grid Array (FBGA/FIBGA) Contact Diameter and Pitch Variations	37
Table 7-3	Comparing Wafer-Level Ball Grid Array (WLBGA) Contact Pitch to Ball or Bump Contact Diameter Range	39
Table 9-1	Typical Feature Sizes for High Density Interconnect (HDI) Substrate Constructions, μm [mil]	52
Table 10-1	Stand-Off Height (SOH) of 0.4-mm Package-on-Package (PoP) With 200- μm Balls	62
Table 12-1	Accelerated Testing for End-Use Environments	74
Table 12-2	Temperature Cycling Requirements, Mandated and Preferred Test Parameters Within Mandated Conditions	75

Design and Assembly Process Implementation of 3D Components

1 SCOPE

This document describes the design and assembly challenges and ways to address those challenges for implementing 3D component technology. Recognizing the effects of combining multiple uncased semiconductor die elements in a single-package format can impact individual component characteristics and can dictate suitable assembly methodology. The information contained in this standard focuses on achieving optimum functionality, process assessment, end-product reliability and repair issues associated with 3D semiconductor package assembly and processing.

1.1 Purpose Performance-driven electronic systems continue to challenge companies in search of more innovative semiconductor package methodologies. The key market driver for semiconductor package technology is to provide greater functionality and improved performance without increasing package size. The package interposer is the key enabler. Although glass-reinforced epoxy-based materials and high-density copper interconnect capability will continue to have a primary role for array-configured packaging, there is a trend toward alternative dielectric platforms as well as toward combining multiple functions within the same die element. To address this movement, an increasing number of semiconductor die developed for advanced applications now require higher I/O with contact pitch variations that are significantly smaller than the mainstream semiconductor products previously in the market. For these applications, companies are developing interposer technologies that can provide interconnect densities far superior to organic-based counterparts.

1.2 Target Audience The target audiences for this standard are managers, design/process engineers and operators who deal with:

- Implementing 3D semiconductor packaging
- Interposer, substrate and PWB design
- Board-level assembly, inspection and repair processes

1.3 Intent This standard intends to provide useful and practical information to those who are designing, developing or using 3D-packaged semiconductor components or those who are considering 3D package implementation. The 3D semiconductor package may include multiple die elements—some homogeneous and some heterogeneous. The package may also include several discrete passive SMT devices, some of which are surface mounted and some of which are integrated (embedded) within the components' substrate structure.

1.4 Definition of Requirements The imperative form of action verbs is used throughout this document to identify acceptance requirements that may require compliance, depending upon the Performance Classification of the hardware (see 12.3). To assist the User, these action verbs are in bold text.

- a) The words **shall/shall not** are used whenever a requirement is intended to express a provision that is mandatory. Deviation from a **shall** or **shall not** requirement for a particular Performance Class may be considered if sufficient technical rationale/objective evidence (OE) is supplied to the User to justify the exception.
- b) The word **should** is used whenever a requirement is intended to express a provision that is nonmandatory and which reflects general industry practice and/or procedure.

1.5 Implementation Challenges The next generation of 3D assembly has many implementation challenges, since the technology is complex and requires process expertise that may require foundries, outsourced semiconductor assembly and test (OSAT) providers and original design manufacturers (ODMs). There is no clear direction where 3D packages will be built, tested and assembled. The type of process to be used and the order of assembly and stacking is not defined and depends on the assembler's expertise.