JEDEC STANDARD

Serial Interface for Data Converters

JESD204C

(Revision of JESD204B.01 January 2012)

DECEMBER 2017

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Foreword

The JESD204 standard separates the communication mechanism between logic devices and data converters into three layers, each with a distinct function: physical (specified in clause 5), link (64B/66B and 64B/80B encoding specified clause 7, and 8B/10B encoding specified in clause 8), and transport (specified in clause 6). The JESD204 physical layer encompasses the PMA and PMD Ethernet layers; the JESD204 link layer encompasses the FEC and PCS Ethernet layers and additional CRC and alignment functionality. Finally, the JESD204 transport layer maps to the MAC Ethernet layer (Figure 1).

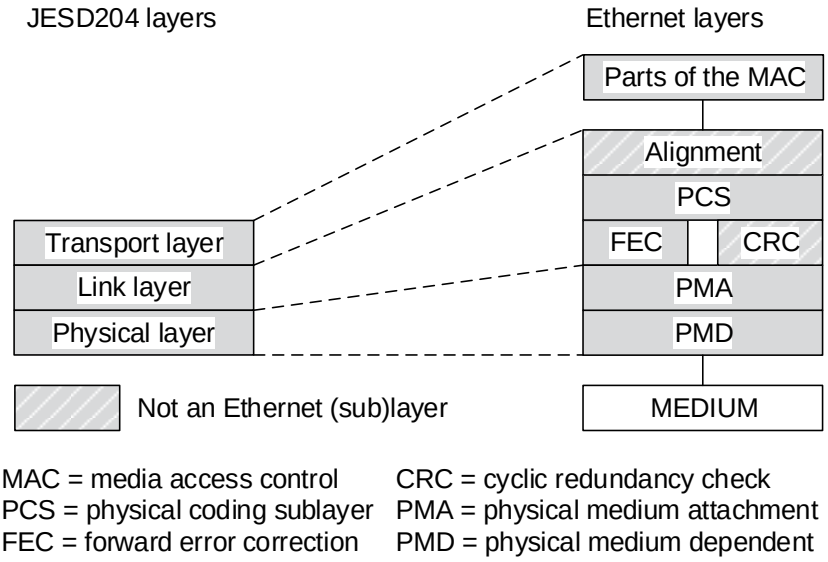

Figure 1 — JESD204 layer relationship to the IEEE Ethernet model

The JESD204C standard replaces the JESD204B standard.

SERIAL INTERFACE FOR DATA CONVERTERS

(From JEDEC Board Ballot JCB-17-43, formulated under cognizance of the JEDEC JC-16 Committee on Interface Technology.)

1 Scope

This standard describes a serialized interface between data converters and logic devices. It contains normative information to enable designers to implement devices that communicate with other devices covered by this specification. Informative annexes are included to clarify and exemplify the document.

Due to the range of applications involved, the intention of this standard is to completely specify only the serial data interface and the link protocol. Certain signals common to both the interface and the function of the device, such as device clocks and control interfaces, have application-dependent requirements. The JESD204 standard does not require a specific implementation of the control interface, however a serial interface is the recommended implementation. Devices may also have application-dependent modes, such as a low power / shutdown mode that will affect the interface. In these instances, the specification merely constrains other device properties as they relate to the interface, and leaves the specific implementation up to the designer.

Revision A of the standard was expanded to support serial data interfaces consisting of single or multiple lanes per converter device. In addition, converter functionality (ADC or DAC) can be distributed over multiple devices:

- All parallel running devices are implemented or specified to run synchronously with each other using the same data format.
- Normally this means that they are part of the same product family.

Revision B of the standard supports the following additional functions:

- Mechanism for achieving repeatable, programmable deterministic delay across the JESD204 link.
- Support for serial data rates up to 12.5 Gbps.
- Transition from using frame clock as the main clock source to using device clock as the main clock source. Device clock frequency requirements offer much more flexibility compared to requiring a frame clock input.

Revision C of the standard now supports the following additional functions:

- Data interfaces up to 32 Gbps.
- Three link layers – 64B/66B, 64B/80B, and 8B/10B. The 8B/10B link layer is similar to the link layer defined in JESD204B.

1 Scope (cont'd)

Figure 2 compares the scope of the original JESD204 specification and its revisions. Although not illustrated in the figure, it is possible to apply multiple, independent instances of the JESD204 standard to the same device. The logic device (e.g., ASIC or FPGA) is always assumed to be a single device.

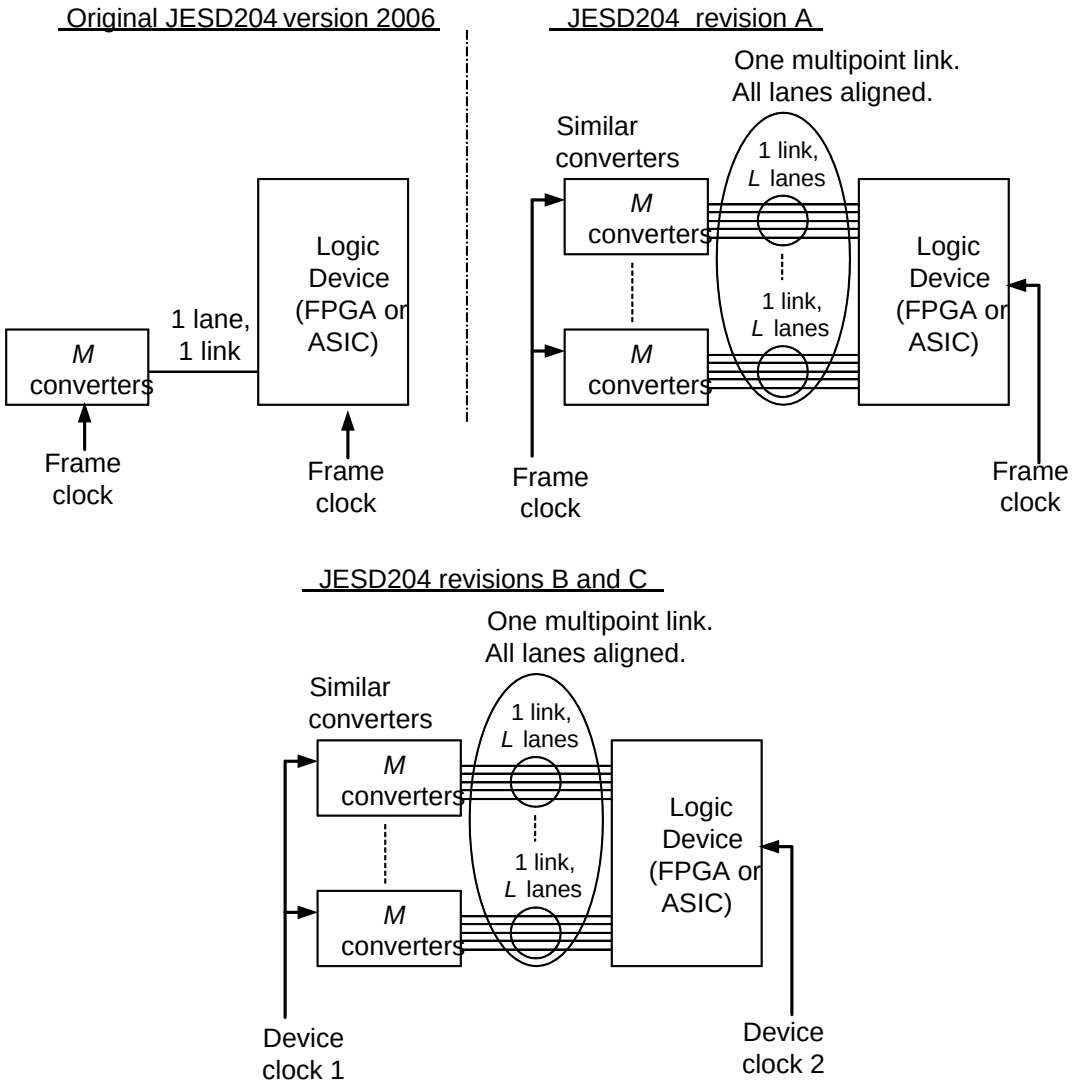

Figure 2 — Scope of original JESD204 and revisions A, B, and C

2 Normative references

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

1. JEDEC JESD99, Terms, Definitions, and Letter Symbols for Microelectronic Devices.

2. IEEE Standard for Ethernet, IEEE Std 802.3™-2015 section 3, clause 36, *Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X*. http://standards.ieee.org/getieee802/.

3. IEEE Standard for Ethernet, IEEE Std 802.3™-2015 section 4, annex 48A, *Jitter test patterns.* http://standards.ieee.org/getieee802/.

4. OIF-SxI-5-01.0, System Interface Level 5 (SxI-5): Common Electrical Characteristics for 2.488 – 3.125 Gbps Parallel Interfaces, Optical Internetworking Forum, October 2002. www.oiforum.com/public/documents/OIF-SxI5-01.0.pdf.

5. OIF-CEI-03.1, Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps and 11G+ bps and 25G+ bps I/O, Optical Internetworking Forum, February 18, 2014 www.oiforum.com/public/documents/OIF_CEI_03.1.pdf.

6. INCITS TR-35-2004 (R2009), Fibre Channel - Methodologies for Jitter and Signal Quality Specification (FC-MJSQ), available from http://webstore.ansi.org.

7. INCITS 450-2009, *Information technology - Fibre Channel - Physical Interface - 4 (FC-PI-4)*, Annex F, *Scrambled test patterns.* Available from http://webstore.ansi.org.

8. INCITS TR-46-2011, *Information technology - Fibre Channel - Methodologies for Signal Quality Specification (FC-MSQS)*, clause 9, *Test patterns*. Available from http://webstore.ansi.org.

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3 Terminology

For the purposes of this standard, the terms and definitions given in JESD204, JESD99 (reference 1), and the following apply:

3.1 Terms and definitions

8B/10B: A DC-balanced octet-oriented data encoding sequence. See IEEE Std 802.3 [**6**].

64B/66B: An encoding type consisting of 64 unaltered user data bits concatenated with a 2 bit sync header. See 7.

64B/80B: An encoding type consisting of 64 unaltered user data bits concatenated with a 2 bit sync header and 14 fill bits. See 7.

active edge of a clock: The clock edge on which the logic changes state.

NOTE 1 The active edge can be the rising edge, the falling edge, or both.

NOTE 2 The drawings in this standard show the rising edge as active edge.

ADC device: A device containing one or more analog-to-digital converters connected to the JESD204 link.

ADC link: A link from an ADC device to a logic device.

analog-to-digital converter: A functional block converting an analog signal to a digital sampled data stream. If the analog signal is converted to a complex data stream, the ADC is defined as the subblock generating either the real or the imaginary component of the data stream.

BERT: Bit Error Ratio Test or Tester (ref. OIF-CEI-03.1).

block (64B/66B or 64B/80B): A structure starting with a 2-bit sync header containing either 66 or 80 bits total.

block (64B/80B): A structure starting with a 2-bit sync header containing 80 bits total.

CDR: Clock Data Recovery (ref. OIF-CEI-03.1).

ceil(x): The smallest integer greater than or equal to x.

character: A symbol produced by 8B/10B encoding of an octet.

NOTE 1 While all octets can be encoded as data characters, certain octets can also be encoded as control characters.

NOTE 2 The same character may exist as two different code groups, depending on running disparity.

3.1 Terms and definitions (cont'd)

clock generator: A circuit used to generate synchronous, phase aligned device clocks to various devices in the JESD204 system.

NOTE A clock generator circuit can include one or more clock generator devices, but they must use a common source clock.

code group: A set of ten bits that, when representing data, conveys an octet. (Applies to 8B/10B encoding, see IEEE Std 802.3 [**6**].)

command channel: Data stream using extra bandwidth afforded from sync headers (see 7.3.7).

control interface: An application-specific interface used to pass information (usually status and control information) between a converter device and a logic device and/or between a device and a higher layer application level.

NOTE The JESD204 specification does not require a specific implementation of the control interface, however a serial interface is the recommended implementation.

converter: An analog-to-digital converter (ADC) or digital-to-analog converter (DAC).

NOTE In this standard, a converter is assumed to interface via a single stream of digital samples.

converter device: A component package containing one or more converters.

NOTE This standard specifies the interactions between one logic device and one or more converter devices.

DAC device: A device containing one or more digital-to-analog converters connected to the JESD204 link.

DAC link: A link from a DAC device to a logic device.

data link: An assembly that is controlled by a link protocol enabling data to be transferred from a data source to a data sink and consists of parts of two devices and the interconnecting data circuit, that is ("terminal" replaced by "device" in Ref. ATIS Telecom Glossary [**1**])

data rate: speed at which data is transferred measured in bits per second, denoted by the symbol f_b.

descrambler: The inverse of a scrambler. (Ref. ATIS Telecom Glossary [**1**])

NOTE The descrambler output is a signal restored to the state that it had when it entered the associated scrambler, provided that no errors have occurred.

device clock: A master clock signal from which a device must generate its local clocks.

digital-to-analog converter: A circuit converting a digital sampled data stream to an analog signal. If the analog signal is converted from a complex data stream, the DAC is defined as the subblock accepting either the real or the imaginary component of the data stream.

EMB_LOCK: A state asserting that extended multiblock alignment has been achieved.

3.1 Terms and definitions (cont'd)

extended multiblock: A set of data containing one or more multiblocks.

fill bit: A bit used to artificially extend the block size in 64B/80B encoding mode.

floor(x): The greatest integer less than or equal to x.

frame: A set of consecutive octets in which the position of each octet can be identified by reference to a frame alignment signal. (Adapted from Ref. ATIS Telecom Glossary).

frame clock: A signal used for sequencing frames or monitoring their alignment.

NOTE A physical frame clock is not required in this version of this standard, but may be required in the implementation of previous versions.

idle mode: An operating mode used for a converter that is not currently sampling data.

invalid code group: A code group that is not found in the proper column of the 8B/10B decoding tables, according to the current running disparity. See IEEE Std 802.3 [**6**].

lane: A differential signal pair for data transmission in one direction.

link: Synonym for "data link".

local clock: A clock derived inside a device from the device clock and used in the

implementation of the JESD204 link within the device.

NOTE 1 It is possible to align a local clock to an external signal, e.g., SYSREF.

NOTE 2 An internal copy of the device clock is not a local clock.

logic device: A component package containing exclusively or primarily digital logic; e.g., an ASIC or FPGA.

NOTE This standard specifies the interactions between one logic device and one or more converter devices.

max(x, y): The largest of x and y.

MB: Multiblock

medium: The transmission path along which a signal propagates.

min(x, y): The smallest of x and y.

mod(x, y): The remainder after dividing x by y (x modulo y).

multiblock: A set of data containing 32 64B/66B or 64B/80B blocks.

3.1 Terms and definitions (cont'd)

multiframe: A set of consecutive frames in which the position of each frame can be identified by reference to a multiframe alignment signal. (Ref. ATIS Telecom Glossary). Applicable to the 8B/10B encoding option, see 8.

NOTE 1 The multiframe alignment signal does not necessarily occur in each multiframe.

NOTE 2 In JESD204, a multiframe consists of *K* frames and is transmitted over a single lane.

multiframe clock: A signal used for sequencing multiframes or monitoring their alignment. Applicable to the 8B/10B encoding option, see 8.

multipoint link: A data communications link that interconnects three or more devices. ("terminal" replaced by "device" in Ref. ATIS Telecom Glossary [**1**].)

nibble: A group of four data bits. (Ref. IEEE 802.3 [**3**])

normal operation: Operation of a link for the purpose of transmitting converter samples. That is, not a test mode or a power down mode.

octet: A group of eight adjacent binary digits (similar to a byte).

receiver: A circuit attached to a lane for reconstructing a serial bit stream into time-aligned frames.

NOTE A receiver consists of one physical layer block and one link layer block.

receiver block: The combination of the receiver transport layer and all receiver link layer and physical layer blocks connected to a link.

receiver device: A component package containing one or more receiver blocks.

relative wander: Components of wander that are uncorrelated between any two in band signals (ref. OIF-CEI-03.1).

rising edge of a differential signal(P,N): The simultaneous transitions that occur when signal(P) changes from the low logic level to the high logic level and signal(N) changes from the high logic level to the low logic level.

running disparity: A binary parameter having a value of + or –, representing the imbalance between the number of ones and zeros in a sequence of 8B/10B code-groups. See IEEE Std 802.3 [**6**].

sample: The instantaneous value of a signal measured or determined at a discrete time. (Adapted from ASIS Telecom Glossary, "sampled data" [**1**].)

NOTE In the context of JESD204, a sample is always the digital representation of a signal.

scrambler: A randomizing mechanism that is used to eliminate long strings of consecutive identical transmitted symbols and avoid the presence of spectral lines in the signal spectrum without changing the signaling rate. (Ref. IEEE 802.3 [**3**])

3.1 Terms and definitions (cont'd)

SH_LOCK: A state that asserts the sync header alignment has been achieved.

skew: The magnitude of the time difference between two events that ideally would occur simultaneously (ref. JESD65B).

steady-state voltage: The voltage at the transmitter output or receiver input resulting from the transmission of a series of consecutive logic-ones or logic-zeros, after the initial transient part of the waveform had ended.

source clock: An oscillator from which the various other clock signals are derived. This oscillator is typically a VCO inside a clock generator device, or an external VCO within a clock generator circuit.

symbol: The smallest unit of coded data on the medium. (Simplified from IEEE 802.3 [**3**])

NOTE In this standard used as synonym to "character".

sync header: Two bits, which guarantee a transition, preceding every block in the 64B/66B and 64/80B link layer (see 7).

sync word: A group of 32 encoded sync transitions in the 64B/66B and 64/80B link layer (see 7).

SYSREF: A periodic, one-shot (strobe-type), or "gapped" periodic signal used to align the boundaries of local clocks in Subclass 1 devices. SYSREF must be source synchronous with the device clock.

transition time: Collective name given to the rise and fall time of a signal.

transmitter: A circuit that serializes the input frames and transports the resulting bit stream across a lane.

NOTE A transmitter consists of one link layer block and one physical layer block.

transmitter block: The combination of the transmitter transport layer and all transmitter link layer and physical layer blocks connected to a link.

transmitter device: A component package containing one or more transmitter blocks.

valid code group: A code group that is found in the proper column of the 8B/10B decoding tables, according to the current running disparity. See IEEE Std 802.3 [**6**].

word: A character string or a binary element string that it is convenient to consider as an entity.

3.2 Symbols and abbreviated terms

$\Delta\boldsymbol{\varepsilon'}$**:** Transmission line dielectric relative permittivity frequency variation magnitude; used in JCOM (see Table 28).

$\Delta\boldsymbol{f}$**:** Frequency step of JCOM (see Table 24).

$\boldsymbol{\varepsilon'_{\infty}}$**:** Transmission line dielectric relative permittivity real part at infinite frequency; used in JCOM (see Table 28).

$\boldsymbol{\eta_o}$**:** One-sided noise spectral density added to received signal after the decision feedback equalizer; used in JCOM (see Table 24).

$\boldsymbol{\sigma_e}$**:** Root-mean-squared error between the measured transmitter steady state output and its linear fit.

$\boldsymbol{\sigma_{RJ}}$**:** Random jitter added to received signal after the decision feedback equalizer; used in JCOM (see Table 24).

/A/: K28.3 character, lane align. Applies to 8B/10B encoding.

$\boldsymbol{a_0}$**:** Intercept of the reference channel length versus maximum channel data rate approximation; used in JCOM (see Table 29)

$\boldsymbol{a_1}$**:** Constant of the inversely proportional to data rate term of the reference channel length versus maximum channel data rate approximation; used in JCOM (see Table 29)

$\boldsymbol{A_{DD}}$**:** Dual-dirac jitter added to received signal after the decision feedback equalizer; used in JCOM (see Table 24).

$\boldsymbol{A_v}$**:** Instantaneous transmitter differential output voltage; used in JCOM (see Table 24).

ADC: Analog-to-Digital Converter

ASIC: Application-Specific Integrated Circuit

B-3: A class of devices that support data rates up to 3.125 Gbps.

B-6: A class of devices that support data rates up to 6.375 Gbps.

B-12: A class of devices that support data rates up to 12.5 Gbps.

$\boldsymbol{b_0}$**:** Intercept of the reference channel differential insertion loss versus maximum data rate linear approximation; used in JCOM (see Table 29).

$\boldsymbol{b_1}$**:** Derivative of the reference channel differential insertion loss versus maximum data rate linear approximation; used in JCOM (see Table 29).

$\boldsymbol{b_{max}(n)}$**:** Normalized maximum decision feedback equalizer coefficient magnitude; used in JCOM (see Table 25).