JEDEC
PUBLICATION

ADAPTER TEST BOARD RELIABILITY TEST GUIDELINES

JEP176

JANUARY 2018

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2018
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

Thomson Reuters

Downloaded by Lewis Poole (lewis.poole@thomsonreuters.com) on Jan 26, 2018, 9:45 am PST

ADAPTER TEST BOARD RELIABILITY TEST GUIDELINES FOR INTEGRATED CIRCUITS

CONTENTS

Introduction

Traditionally, integrated circuits packaged in through-hole packages and surface mount packages can be placed directly into Automatic Test Equipment (ATE) for electrical test for reliability tests and production. However, for solder-bump-based packages, this test method becomes challenging. One alternative method of performing electrical tests and reliability tests is to mount integrated circuits in solder bump-based-packages onto adapter test boards, which enables the connection between the integrated circuit devices to the biased reliability boards and ATE. Chip-Scale Packages (CSP), Flip-Chip Die that are to be assembled directly to boards, and other Fine-Pitch Packages (FPP) may benefit from use of an electrical test adapter board for component-level reliability testing.

This document provides guidelines on testing of integrated circuit devices mounted on adapter test boards specifically for the purpose of performing reliability tests to identify component-level failure mechanisms. The use of adapter test boards is a lower cost alternative to using custom sockets on the biased reliability boards and ATE interface boards.

This publication recommends that JESD47 or another JEDEC qualification standard be used. This document augments those requirements with guidance on some testing that may be preferable to execute in a format where the supplied device is mounted on an adapter test board either for the purpose of handling efficiency through the reliability stress or electrical test evaluations. The reliability stress test is performed to assess the robustness of the chip-scale, flip-chip, and fine-pitch package manufacturing process and/or to determine whether there are chip-package interaction effects. These considerations apply to devices in chip-scale packaging, flip-chip direct attach, and fine-pitch packages. This document also offers guidelines for mitigating the risk of adapter test-board-related failure mechanisms.

ADAPTER TEST BOARD RELIABILITY TEST GUIDELINES

(From JEDEC Board Ballot JCB-17-36, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

This publication describes guidelines for applying JEDEC reliability tests and recommended testing procedures to integrated circuits that require adapter test boards for electrical and reliability testing. These tests are used frequently in qualifying integrated circuits as a new product, a product family, or as products in a process which is being changed.

Integrated circuit devices in various packages that cannot be tested directly with the Automated Test Equipment (ATE) are each mounted on an adapter test board for testing. Some common devices mounted on adapter test boards for test purposes are Chip-Scale Package, Flip-Chip Die, and Fine-Pitch Package devices (e.g., 64-Lead QFN package with 0.50-mil lead pitch).

This document provides guidelines for adapter test board-level reliability tests, recommended testing procedures, test board designs, and construction materials. It is aimed to provide a reproducible assessment of the reliability performance of integrated circuit devices while duplicating the failure modes normally observed during product life cycle. The reliability test recommendations do not apply to the following:

a) Integrated circuits that are stressed and/or tested in an electrical socket.
b) WLCSP devices that are stressed and/or tested using a wafer-level probe card.
c) Second-level solder joint reliability tests such as drop test, thermal cycle test, bend test, etc.

These reliability tests are capable of evaluating and simulating package and device failures in an accelerated manner compared to use conditions. The guidelines prescribed in this publication are not aimed for reliability tests for devices in extreme use conditions such as military applications, automotive under-the-hood applications, or uncontrolled avionics environments. Each reliability test should be examined for:

a) Any potential new and unique failure mechanisms,
b) Any situation where these tests and/or conditions may induce false failures.