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BSI Standards Publication

Semiconductor devices - Scan based ageing level estimation for semiconductor devices

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National foreword

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A list of organizations represented on this committee can be obtained on request to its secretary.

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TECHNICAL REPORT

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Semiconductor devices –
Scan based ageing level estimation for semiconductor devices

INTERNATIONAL
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COMMISSION

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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FOREWORD

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IEC TR 63133, which is a technical report, has been prepared by IEC technical committee 47: Semiconductor devices.

The text of this technical report is based on the following documents:

Enquiry draft	Report on voting
47/2405/DTR	47/2425/RVDTR

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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INTRODUCTION

A semiconductor device has an important role in reliability-critical applications, e.g., space, air and road vehicles, medical equipment. Although new technology has improved performance, power efficiency, cost efficiency etc., but the reliability becomes a serious threat [1][1]. As can be seen in Figure 1, failure rate is decreases in early life, and low constant failure rate is preserved for a while, then wear out failure rate is increases significantly. Especially for reliability-critical applications, it is important to precisely monitor the ageing level to forewarn of any impending catastrophic failure. The semiconductor ageing is caused by negative/positive bias temperature instability, hot carrier injection, and time dependent dielectric breakdown, electro migration, and stress migration, etc. Path delay is known to be increased due to various ageing failures. Although a few ageing monitoring techniques have been developed [2 to 5], the ageing level has not been precisely diagnosed. For reliability-critical applications, the ageing level information can be utilized for taking adequate measures timely, e.g., device replacement, performance switching using dynamic voltage-frequency scaling. This document describes an efficient technique to monitor the ageing and characterize the ageing level.

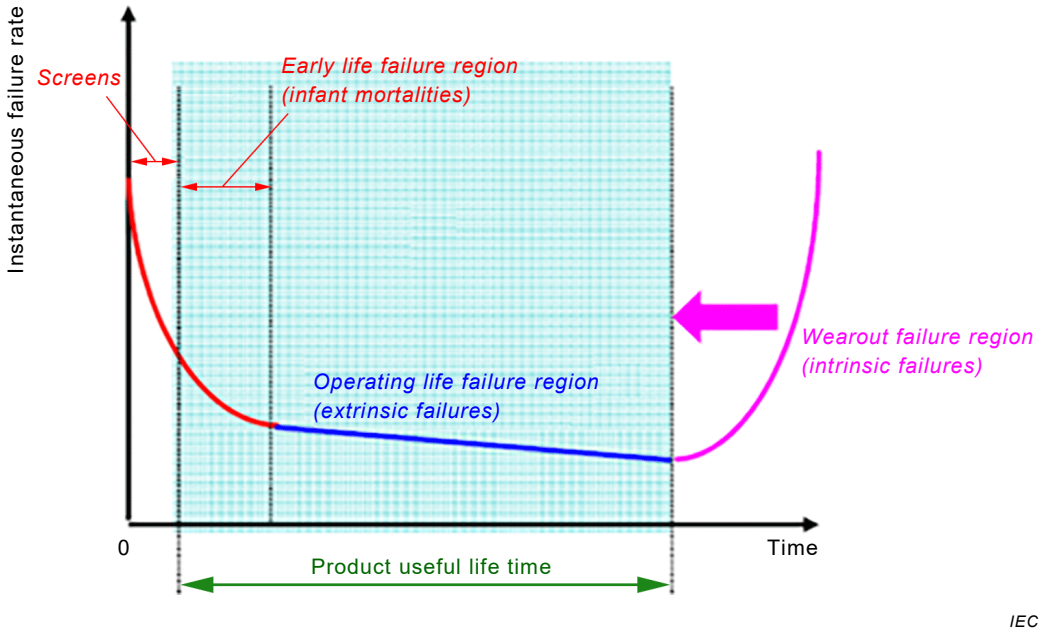

Figure 1 – Reliability bathtub curve

1 Numbers in square brackets refer to the Bibliography.

SEMICONDUCTOR DEVICES –

Scan based ageing level estimation for semiconductor devices

1 Scope

This Technical Report specifies a design technique of performance estimation storage element, which can monitor semiconductor ageing and characterize ageing level. The estimated ageing level can be used to improve the reliability of system.

2 Normative references

There are no normative references in this document.

3 Terms, definitions and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
  ISO Online browsing platform: available at http://www.iso.org/obp

3.1.1
transistor ageing
for a field effect transistor, increase with time of its threshold voltage

Note 1 to entry: This increase is caused by a combination of NBTI, PBTI, HCI, TDDB, EM, and SM.

Note 2 to entry: This effect decreases the drain current and transconductance and thereby increases the path delay.

3.1.2
ageing level
degree of transistor ageing under known operating conditions

3.1.3
ageing level monitoring
method of evaluating transistor ageing that indicates either pass or fail at a selected ageing level

Note 1 to entry: The amount of delay between two clock signals corresponds to the selected ageing level.

Note 2 to entry: A path delay longer than the clock delay plus guard band constitutes a failure.

3.1.4
guard band
timing margin that allows for the worst acceptable increase of path delay through a device