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Chip-Package Interaction Understanding, Identification, and Evaluation

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CHIP-PACKAGE INTERACTION UNDERSTANDING, IDENTIFICATION, AND EVALUATION

Introduction

The present solid state component level test structures or procedures do not always ensure that problems associated with chip-package interactions (CPI) are discovered in standard device level qualifications. As component structures integrate ultra low-k (ULK) chip level dielectrics to increase performance, the interaction between the device and the package increases, though these interactions can be found in prior technologies. This document discusses identification and evaluation methods to evaluate the effect of chip package interactions on product reliability.

CHIP-PACKAGE INTERACTION UNDERSTANDING, IDENTIFICATION AND EVALUATION GUIDELINE

(From JEDEC Board Ballot JCB-18-12, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

This publication references a set of frequently recommended and accepted JEDEC reliability stress tests. These tests are used for qualifying new and modified technology/ process/ product families, as well as individual solid state surface-mount products. CPI test structures may not be a prerequisite for device qualification dependent on the device technology; however, if the effect of CPI on a device technology placed in a specific packaging scheme is not known, there could be reliability concerns for that component that are not evident with standard component level test structures. Therefore, it is recommended that CPI test structures are used and the associated testing and failure analysis be performed to determine if there are any adverse effects on that component due to packaging. Chip sizes and packages should be used that are representative of the product family to allow investigation of failure mechanisms for those products.

NOTE This publication covers only interaction between the semiconductor package stresses and the semiconductor device. Interactions between the assembled component and a second level assembly are not covered. See JEP 150 for information regarding assembled component reliability. Interactions resulting from package interconnect electromigration are also not covered. See JEP 154 regarding Package interconnect electromigration. . See JEP158 for the effects on chip reliability due to through-silicon vias (TSVs).

NOTE CPI tests should be performed in addition to process and package qualification typically performed on new products.

These reliability stress tests have been found capable of stimulating and precipitating failures in components in an accelerated manner, but these tests should not be used indiscriminately. Each qualification should be examined for:

- a) Any potential new and unique failure mechanism
- b) Any situations where these tests/conditions may induce invalid or overstress failures.

In either case the set of reliability requirements, tests and/or conditions should be appropriately modified to properly include the new failure mechanisms and modes.

This document does not relieve the supplier of the responsibility to meet internal or customer specified qualification programs.