JEDEC STANDARD

DDR4 NVDIMM-N Design Specification

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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DDR4 NVDIMM-N DESIGN SPECIFICATION

(From JEDEC Board Ballot JCB-17-40, formulated under the cognizance of the JC-45.6 Subcommittee on Hybrid Modules.)

1 Scope

This standard defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Double Data Rate, Synchronous SDRAM Non-Volatile Dual In-Line Memory Modules with NAND Flash backup (DDR4 NVDIMM-N). A DDR4 NVDIMM-N is a Hybrid Memory Module with a DDR4 DIMM interface consisting of DRAM that is made non-volatile through the use of NAND Flash. NVDIMM-N modules adhere to the Byte Addressable Energy Backed Interface specification.

The JESD245B Byte Addressable Energy Backed Interface specification provides detailed logical behavior, interface, and register definitions. These DDR4 NVDIMM-N's are intended for use as persistent memory when installed in PCs.

An NVDIMM-N is either an:

- NVLRDIMM-N: a Load Reduced DIMM (LRDIMM) compliant with JESD21C Page 4.20.27 *DDR4 SDRAM Load Reduced DIMM Design specification* except as specified in this standard; or
- NVRDIMM-N: a Registered DIMM (RDIMM) compliant with JESD21C Page 4.20.28 *DDR4 SDRAM Registered DIMM Design Specification* except as specified in this standard.

System interface constraints are included which provide an initial basis for DDR4 NVDIMM-N designs. Modifications to these constraints may be required to meet all system timing, signal integrity and thermal requirements for PC4-1600, PC4-1866, PC4-2133, PC4-2400, PC4-2666 and PC4-3200 support. All DDR4 NVDIMM-N implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

The annex for each raw card will have specific entries to indicate DIMM operation and voltage levels. This specification works in conjunction with:

- JESD21C, Page 4.1.2.L-5 *Annex L: Serial Presence Detect (SPD) for DDR4 SDRAM Modules (DDR4 SPD Document Release 5)*
- JESD21C, Page 4.20.27 *DDR4 SDRAM Load Reduced DIMM Design Specification* (August 2015)
- JESD21C, Page 4.20.28 *DDR4 SDRAM Registered DIMM Design Specification* (August 2015)
- JESD79-4B, *DDR4 SDRAM* (June 2017)
- JESD245B, *Byte Addressable Energy Backed Interface* (July 2017)

1 Scope (cont'd)

Table 1 — DDR4 Product Family Attributes

DIMM Organization	x72 ECC	Notes
DIMM Dimensions (nominal)	133.35 mm x 31.25 mm	Refer to MO-309
	133.35 mm x 18.75 mm	Refer to MO-309
Pin Count	288	
DDR4 SDRAMs Supported	4Gb, 8Gb, 16Gb	78/106-ball FBGA package for x4 and x8 devices. Refer to MO-207: variations DT-z, DW-z
Capacity	4GB, 8GB, 16GB, 32GB, 64GB, 128GB	
SDRAM width	x4, x8	
Serial Presence Detect, Thermal Sensor (SPD-TSE)	512 byte	TSE2004av specifications
Voltage Options	VDD: PC4 - 1.2 Volt ±5%, PC4L - TBD	
	VPP: 2.5 Volt +10%, -5%	The VPP supply has VSS as its return path. VPP is a separate supply.
	VDDSPD: 2.5 Volt ±10%	The VDDSPD supply has VSS as its return path. VDDSPD is separate from the VPP power plane. VDDSPD is shared between the SPD-TSE and the RCD (register). The RCD only supports 2.5V.
	V_12: +12 Volt ±15%	The +12 V supply has VSS as its return path. +12 V is required for NVDIMM-N operation.
Interface	1.2 V signaling	

2 Environmental Requirements

288-pin Registered DDR4 NVDIMM-N modules are intended for use in a variety of environments including standard office environments that have limited capacity for heating and air conditioning.

Table 2 — Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +55	°C	3
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
T_{STG}	Storage Temperature	-50 to +100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The component maximum case temperature (T_{CASE}) shall not exceed the value specified in the DDR4 SDRAM component specification.