JEDEC STANDARD

POD135 - 1.35 V Pseudo Open Drain I/O

JESD8-21B

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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POD135 - 1.35V PSEUDO OPEN DRAIN I/O

(From JEDEC Board Ballot JCB-18-01, formulated uder the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the dc and ac single-ended (data) and differential (clock) operating conditions, I/O impedances, and the termination and calibration scheme for 1.35V Pseudo Open Drain I/Os. The 1.35V Pseudo Open Drain interface, also known as POD135, is primarily used to communicate with GDDR5 or GDDR5M SGRAM devices.

Multiple Classes of POD135 are expected to reside within the family of POD135 interfaces in order to accommodate various device and market applications. The various classes standardized within the context of POD135 are documented in the appendices of this document (e.g., POD135/Class A, POD135/Class B, etc).

The core of this standard defines documents the subset of values common to all Classes of POD135 and documents specification items left to definition within a specific Class as denoted by CDV which is defined as Class Dependent Value.

The values specific to each particular class of POD135 are found in the annexes. See specific Class tables for further details. (Note it does not follow that all specification values defined in a given Class are necessarily different from the matching parameter in other Class within POD135. Multiple Classes may reuse a given specification value if appropriate to the Class requirements.)

Classes were not part of the original POD135 specification. With the addition of Classes the original POD135 values remain unchanged and grouped as POD135/Class A and POD135/Class C. The updates to the specification are included in POD135/Class B and POD135/Class D. As other devices or market applications are defined, they may use one of the already defined Class(es) or define a new Class.

2 Core POD135 Interface Standard

Table 1 — DC Operating Conditions

		POD135				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
Device Supply Voltage	VDD	1.3095	1.35	1.3905	V	1
Output Supply Voltage	VDDQ	1.3095	1.35	1.3905	V	1
Reference Voltage	VREF	CDV		CDV	V	2, 6
Reference Voltage for DQ and DBI_n pins	VREFD	CDV		CDV	V	2, 7
Reference Voltage for DQ and DBI_n pins	VREFD2	CDV		CDV	V	2, 7
External Reference Voltage for address and command	VREFC	CDV		CDV	V	3, 7
DC Input Logic HIGH Voltage	VIH (DC)	CDV			V	6
DC Input Logic LOW Voltage	VIL (DC)			CDV	V	6
DC Input Logic HIGH Voltage for address and command	VIHA (DC)	CDV			V	7
DC Input Logic LOW Voltage for address and command	VILA (DC)			CDV	V	7
DC Input Logic HIGH Voltage for DQ and DBI_n pins with VREFD	VIHD (DC)	CDV			V	7
DC Input Logic LOW Voltage for DQ and DBI_n pins with VREFD	VILD (DC)			CDV	V	7
DC Input Logic HIGH Voltage for DQ and DBI_n pins with VREFD2	VIHD2 (DC)	CDV			V	7
DC Input Logic LOW Voltage for DQ and DBI_n pins with VREFD2	VILD2 (DC)			CDV	V	7
Input Logic HIGH Voltage for RESET_n, SEN, MF	VIHR	CDV			V	7
Input Logic LOW Voltage for RESET_n, SEN, MF	VILR			CDV	V	7
Input logic HIGH voltage for EDC1/2 (x16 mode detect)	VIHX	CDV			V	7
Input logic LOW voltage for EDC1/2 (x16 mode detect)	VILX			CDV	V	7
Input Leakage Current Any Input 0V <= V_{IN} <= VDDQ (All other pins not under test = 0V)	Il				µA	
Output Leakage Current (DQs are disabled; 0V <= Vout <= VDDQ)	Ioz				µA	
Output Logic LOW Voltage	VOL (DC)			0.56	V	

NOTE 1 GDDD5 SGRAM devices are designed to tolerate PCB designs with separate VDD and VDDQ power regulators.
NOTE 2 AC noise in the system is estimated at 50mV pk-pk for the purpose of DRAM design.
NOTE 3 External VREFC is to be provided by the controller as there is no other alternative supply.
NOTE 4 DQ/DBI_n input slew rate must be greater than or equal to 2.7V/ns. The slew rate is measured between VREFD crossing and VIHD(AC) or VILD(AC) or VREFD2 crossing and VIHD2(AC) or VILD2(AC).
NOTE 5 ADD/CMD input slew rate must be greater than or equal to 2.7V/ns. The slew rate is measured between VREFC crossing and VIHA(AC) or VILA(AC).
NOTE 6 Applicable to an interface with a single VREF for the device.
NOTE 7 Applicable to an interface with multiple VREF pins and levels