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Recommended ESD Target Level for HBM Qualification

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Contents

Foreword ... **ii**
Introduction ... **ii**
1 Scope ... **1**
2 References ... **1**
3 Terms, definitions, and letter symbols ... **4**
4 Historical Perspective on HBM/MM ESD Requirements ... **5**
4.1 Motivation for the HBM Target Level ... 5
4.2 Motivation for Introducing Machine Model (MM) ... 5
5 Changes and Improvements in ESD and Control Environment ... **6**
5.1 Historic ESD Handling Procedures ... 6
5.2 Global Implementation of ESD Control ... 7
5.2.1 Ground and Bond all Conductors: ... 8
5.2.2 Control Charges on Insulators ... 8
5.2.3 Use Protective Packaging for Transit and Storage ... 8
5.2.4 ESD Control Programs and Resulting Data ... 9
5.2.5 Advantage of Process Analysis ... 10
5.3 Change of HBM Hazard Scenario by Increasing the Automation Level ... 12
6 Consolidated Industry Data on HBM Levels vs. Field Returns ... **13**
6.1 Field Return Rates versus HBM Level ... 13
6.2 Case Studies ... 16
6.2.1 Devices with Failure Levels below 500 V HBM ... 16
6.2.2 Devices that Fail between 500-1000 V HBM ... 16
6.2.3 Devices that Fail between 1000-2000 V HBM ... 17
6.3 Conclusion ... 17
7 Impact of ESD Requirements from Customers and Suppliers ... **18**
7.1 ESD Requirements and Specification Failures ... 18
7.2 Impact of "ESD Failures" ... 18
7.3 Impact of a Revised ESD Target Level ... 20
8 IC Technology Scaling Effects on Component Level ESD ... **21**
8.1 Scaling Effects on ESD Robustness ... 21
8.2 Protection Design Window ... 24
8.3 ESD Capacitive Loading Requirements ... 26
8.4 Package Effects ... 29
8.5 ESD Technology Roadmap ... 30
8.6 Discussion ... 31
9 Differences between Component ESD and System Level ESD ... **32**
9.1 The History of System Level ESD ... 32
9.2 Differences in Component and System Level ESD Stress Models ... 32
9.3 Case Studies ... 34
9.4 Conclusion ... 34
10 Recommendations for a New ESD Target Level ... **35**
10.1 New Realistic Target Level for HBM ... 35
10.2 Treatment of Special Pins ... 36
10.3 Timeframe for Applying New Recommendations ... 36
10.4 Future Cost of ESD Design ... 36
10.5 Product ESD Evaluation Criteria ... 37
10.6 Looking Forward ... 38
Annex A (informative) Frequently Asked Questions ... **39**
Annex B (informative) Machine Model – Correlation between HBM and MM ESD ... **44**
B.1 Correlation: HBM vs. MM ... 44
B.1.1 Consequence of 1 kV HBM Target ... 45
B.2 Exceptions to HBM/MM Ratio ... 47
B.2.1 Bipolar vs. Unipolar Stress ... 47
B.2.2 Advanced Technologies ... 48
B.3 Conclusions ... 49
Annex C (informative) Differences between JEP155B and JEP155A.01 ... **50**

RECOMMENDED ESD TARGET LEVEL FOR HBM QUALIFICATION

Foreword

For more than 20 years, IC component level ESD target levels for both HBM (2 kV) and MM (200 V) have essentially stayed constant, with no focus on data to change these levels. Today's enhanced static control methods required by OEMs do not justify these higher HBM/MM levels as data will show in this document. ESD over-design to these levels in today's latest silicon technologies is increasingly constraining silicon area as well as performance, and is leading to more frequent delays in the product innovation cycle. Based on improved static control technology, field failure rate, case study and ESD design data, collected from IC suppliers and contract manufacturers, we propose a more realistic and safe HBM ESD target level which ensures a minimum MM performance level. This new HBM level (1 kV HBM) is easily achievable with static control methods mandated by customers and with today's modern ESD design methods. As discussed in JEP172, MM testing is redundant to HBM and produces the same failure mechanisms. As a result, target level discussions for MM have been removed from this document as they are not applicable in component level testing (see JESD47 [1]). In addition, Clause 6 from the first revision of this document has been moved to Annex B. This is to preserve the data for future reference.

Introduction

This document was written with the intent to provide information for quality organizations in both semiconductor companies and their customers to assess and make decisions on safe ESD level requirements. It will be shown through this document why realistic lowering of the ESD target level for HBM component level ESD is not only essential but is also urgent. The document is organized in different sections to give as many technical details as possible to support the purpose given in the abstract. Additionally, frequently asked questions (FAQ) in the annex are intended to avoid any misconceptions that commonly occur while interpreting the data and the conclusions herein. All component level ESD testing specified within this document adheres to the methods defined in the appropriate JEDEC and ESDA/ANSI specifications.

In June 2009, the formulating committee unanimously approved the addition of the ESDA logo on the covers of this document.

Since the first release of JEP155, additional work has been completed to show that MM qualification testing is not needed. This has been released as a separate JEDEC publication, JEP172 [2]. MM qualification testing is not a required component level qualification test per JEDEC (see JESD47 [1]), EOS/ESD Association, AEC and JEITA. HBM and CDM testing are sufficient component level qualification tests to assess IC ESD robustness. In response to JEP172, this update to JEP155 will remove references to MM qualification testing, with Clause 6 being moved to Annex B. It should be noted that this discussion is only for MM *qualification testing*, this does not imply that there are no risks in an ESD protected area (EPA) due to isolated conductors. The Industry Council recommends an appropriate ESD control program is put in place as per ANSI/ESD S20.20 or IEC 61340-5-1 in order to ensure low risk to isolated conductors. An assessment of MM performance can be determined by the HBM qualification test data as discussed in Annex B.

It should be noted that several figures related to technology nodes are from the initial release of the publication. While the data is older, the trends and conclusions from that data still hold true today.

RECOMMENDED ESD TARGET LEVEL FOR HBM QUALIFICATION

(From JEDEC Board Ballot JCB-18-14, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

The intent of this report is to document and provide critical information to assess and make decisions on safe ESD level requirements. The scope of this document is to provide this information to quality organizations in both semiconductor companies and their IC customers.

1.1 Special Notes on the System Level ESD:

1. This work and the recommendations therein are intended for Component Level safe ESD requirements and will have little or no effect on system level ESD results.
2. Systems and System boards should continue to be designed to meet appropriate ESD threats regardless of the components in the systems that are meeting the new recommendations from this work, and that all proper system reliability must be assessed through the IEC test method.

1.2 Special Notes on the Machine Model:

1. The machine model (MM) method as specified by some customers and suppliers is not a qualification methodology by JEDEC for use in place of or in addition to HBM and CDM test qualification.

2 References

[1] JEDEC Standard JESD47, “Stress-Test-Driven Qualification of Integrated Circuits”, www.jedec.org

[2] JEDEC Publication JEP172, “Discontinuing Use of the Machine Model for Device ESD Qualification”, www.jedec.org

[3] W.M. King, “Dynamic waveform Characteristics of Personnel Electrostatic Discharge”, EOS/ESD Symposium Proceedings, EOS-1, 78 (1979).

[4] L. Avery, private communication.

[5] D.L. Lin, M.S. Strauss, and T.L. Welsher, “On the Validity of ESD Threshold Data Obtained Using Commercial Human-Body Model Simulators”, Proceedings of the 25th International Reliability Physics Symposium, 77 (1987).

[6] M.S. Strauss, D.L. Lin, and T.L. Welsher, “Variations in Failure Modes and Cumulative Effects Produced aby Commercial Human-Body Model Simulators”, EOS/ESD Symposium Proceedings, EOS-9, 59-63 (1987).

[7] ANSI/ESD S20.20-2014; Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)

[8] IEC 61340-5-1; Electrostatics – Part 5: Specification for the protection of electronic devices from electrostatic phenomena – Section 1: General requirements; 12.1998