JEDEC STANDARD

Stress-Test-Driven Qualification of Integrated Circuits

JESD47K

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STRESS DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS

Contents

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(From JEDEC Board Ballot, JCB-18-25, formulated under the cognizance of the JC14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

This standard describes a baseline set of acceptance tests for use in qualifying electronic components as new products, a product family, or as products in a process which is being changed.

These tests are capable of stimulating and precipitating semiconductor device and packaging failure modes on free-standing components not soldered to a printed wired board (PWB), or the like (base component reliability). The objective is to precipitate failures in an accelerated manner compared to use conditions. Failure Rate projections usually require larger sample sizes than are called out in qualification testing. For guidance on projecting failure rates, refer to JESD85 Methods for Calculating Failure Rates in Units of FITs.

This qualification standard is aimed at a generic qualification for a range of use conditions, but

- may not be applicable at extreme use conditions such as military applications, automotive under-the-hood applications, or uncontrolled avionics environments
- does not cover components assembled onto a PWB, or the like, which may affect the component reliability under assembled state. This is addressed in JEP150 and e.g., typically applies to TC on WLCSP devices

Additional qualification testing tailored to meet specific requirements such as solder joint interconnect reliability can be developed by applying JESD94.

This set of tests should not be used indiscriminately. Each qualification project should be examined for:

a) Any potential new and unique failure mechanisms.
b) Any situations where these tests/conditions may induce invalid or overstress failures.

If it is known or suspected that failures either are due to new mechanisms or are uniquely induced by the severity of the test conditions, then the application of the test condition as stated is not recommended. Alternatively, new mechanisms or uniquely problematic stress levels should be addressed by building an understanding of the mechanism and its behavior with respect to accelerated stress conditions (Ref. JESD91, “Method for Developing Acceleration Models for Electronic Component Failure Mechanisms” and JESD94, “Application Specific Qualification using Knowledge Based Test Methodology”).

Consideration of PC board assembly-level effects may also be necessary. For guidance on this, refer to JEP150, Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components.

This document does not relieve the supplier of the responsibility to assure that a product meets the complete set of its requirements.