# JEDEC STANDARD

# Serial Flash Discoverable Parameters (SFDP)

# JESD216C

(Revision of JESD216B, May 2014)

**AUGUST 2018**

**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**

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Published by
©JEDEC Solid State Technology Association 2018
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2108



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Printed in the U.S.A.

# SERIAL FLASH DISCOVERABLE PARAMETERS (SFDP) STANDARD

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## Foreword

This standard was prepared by the JEDEC SFDP Task Group authorized by the JC-42.4 Committee Chairman

The intended audience is serial flash vendors and engineers writing device drivers for SFDP compliant serial flash devices.

The participating SFDP TG members included volunteers from Adesto, Cypress, Giga Device, Intel, ISSI, Macronix, Micron, Microchip, NXP, Sanyo, and Winbond.

## Introduction

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors.

The SFDP standard defines a common parameter table describing important device characteristics and serial access methods used to read the parameter table data. Optional Special Function parameter tables for erase sector address map and 4-byte address instructions are included. New in the JESD216C revision are optional Special Function parameter tables for the JEDEC eXtended Serial Peripheral Interface (xSPI) and for the Status, Control and Configuration Register Map for SPI Memory Devices. Additional parameter headers and tables can be specified by future revisions of this standard or by flash vendors and are optional.

# SERIAL FLASH DISCOVERABLE PARAMETERS (SFDP) STANDARD

(From JEDEC Board Ballot JCB-18-02, formulated under the cognizance of the JC-42.4 Committee on Nonvolatile Memory.)

## 1 Scope

The SFDP standard defines the structure of the SFDP database within the memory device and methods used to read its data.

The JEDEC-defined header with Parameter ID FF00h and the related Basic Parameter Table is mandatory. This header and table provide basic information for a Serial Peripheral Interface (SPI) protocol memory. Additional headers and tables are optional.

The read command protocol using various I/O modes and standard clock rate are specified. The device electrical parameters are not specified.

## 2 Normative reference

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents listed. For undated references, the latest edition of the normative document referred to applies.

1. JEP106, *Standard Manufacturers Identification Code* (see www.jedec.org for latest revision)

2. NIST SP800-147, *BIOS Protection Guidelines* (http://nvlpubs.nist.gov/nistpubs/Legacy/SP/nistspecialpublication800-147.pdf)

3. JEDEC Standard JESD251, *eXpanded Serial Peripheral Interface (xSPI) for Non Volatile Memory Devices* as approved by JC42.4 committee in the June 2017 meeting.

   JEDEC Standard JESDxxx, *SPI Protocol Reset (Serial Peripheral Interface - Flash Hardware Reset Method, Not Requiring a Dedicated Reset Signal Input,* **This document in development.**

4. JEDEC Standard JESD230C, *NAND Flash Interface Interoperability*