JEDEC STANDARD

Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Stress Test

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JEDEC Solid State Technology Association

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ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM / ERASE ENDURANCE AND DATA RETENTION STRESS TEST

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Foreword

This reliability test is intended to determine the ability of an “EEPROM” integrated circuit or an integrated circuit with an “EEPROM” module (such as a microprocessor) to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life of the “EEPROM” (data retention).

ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM/ERASE ENDURANCE AND DATA RETENTION STRESS TEST

(From JEDEC Board Ballot JCB-18-20, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods and Packaged Devices.)

1 Scope

This standard specifies the procedural requirements for performing valid endurance and retention tests based on a qualification specification. Endurance and retention qualification specifications (for cycle counts, durations, temperatures, and sample sizes) are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

The program/erase endurance and data retention test for qualification and monitoring, using the parameter levels specified in JESD47, is considered destructive. The data retention stress may be used as a proxy to replace the high temperature storage life test when the temperature and time meet or exceed qualification requirements. Lesser test parameter levels (e.g., of temperature, number of cycles, retention bake duration) may be used for screening as long as these parameter levels have been verified by the device manufacturer to be nondestructive; this can be performed anywhere from wafer level to finished device.

2 Terms and definitions

For the purpose of this publication, the following terms and definitions apply.

data pattern: The mix of 1s and 0s in the memory and their physical or logical positions.

NOTE A device may be single-bit-per-cell (SBC), meaning that one physical memory cell stores a “0” or a “1”, or multiple-bits-per-cell (MBC), meaning that one cell stores two or more bits of data: “00”, “01”, “10”, or “11”. In some MBC memories, the two bits represent logically-adjacent bit-pairs in each byte of data. For example, a byte containing binary data 10110001 would correspond to four physical cells with data 2301 in base-four logic. In other MBC memories, the two bits may represent bits in entirely different address locations. For an SBC memory a physical checkerboard pattern consists of alternating 0s and 1s, with each 0 surrounded by 1s on either side and above and below; a logical checkerboard pattern consists of data bytes AAH or 55H in which each 0 is logically adjacent to 1s. In some qualifications only logical positions may be known.

data retention; retention: The ability of an EEPROM cell to retain data over time.

NOTE 1 The one-word term “retention” is usually used when context ensures that no confusion is likely; otherwise, the full term “data retention” should be used.

NOTE 2 The term “data retention” may refer to the ability of a device to retain data in the unbiased state, but the term will sometimes be used to include the ability to retain data under bias. The term “disturb” refers unambiguously to the ability of an ”EEPROM” cell to retain data over time under bias. For example, read “disturb” refers to the ability of an “EEPROM” cell to retain data after being read a given number of times. A detailed discussion of “disturb” is beyond the scope of this document.

NOTE 3 Retention stressing consists of writing a data pattern into a device and then verifying that the pattern is intact after a specified time at a specified temperature. There is no single data pattern that is worst-case for all “retention” mechanisms, cell designs, or process architectures. There are generally some failure mechanisms that primarily affect programmed cells and some that primarily affect erased cells, and there are also failure mechanisms that depend on the data in adjacent cells.