IPC/PERM-WP-022

2018 - August

Mitigation of Pure Tin Risk by Tin-Lead SMT Reflow – Results of an Industry Round-Robin – Final Report

A White Paper Report Developed by IPC

Association Connecting Electronics Industries

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Developed by the PERM Self-Mitigation of Tin By SMT Task Group (8-81) of the Pb-Free Electronics Risk Management (PERM) Council (8-80) and IPC

Users of this publication are encouraged to participate in the development of future revisions.

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Acknowledgment

Any document involving a complex technology draws material from a vast number of sources across many continents. While the principal members of the PERM Self-Mitigation of Tin By SMT Task Group (8-81F) of the PB-free Electronics Risk Management (PERM) Council (8-80) are shown below, it is not possible to include all of those who assisted in the evolution of this white paper. To each of them, the members of the IPC extend their gratitude.

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Abstract

The risk associated with whisker growth from pure tin solderable terminations is fully mitigated when all of the pure tin is dissolved into tin-lead solder during SMT reflow. In order to take full advantage of this phenomenon, it is necessary to understand the conditions under which such coverage can be assured. A round robin study has been performed by IPC/PERM Task group 8-81, during which identical sets of test vehicles were assembled, in accordance with IPC J-STD-001, Class 3, at multiple locations. All of the test vehicles were analyzed to determine the extent of complete tin dissolution on a variety of component types. Results of this study are presented together with relevant conclusions and recommendations to guide high reliability end-users on the applicability and limitations of this mitigation strategy.

Background

Manufacturers of high reliability electronics have been working for many years to mitigate the deleterious effects of tin whisker formation. One highly effective means to suppress the growth of tin whiskers is to replace the pure tin plating with reflowed tin-lead solder. (This approach is only available to manufacturers whose products are not subject to Restrictions of Hazardous Substances (RoHS)). One approach to achieve total replacement of tin plating with tin-lead solder is to perform a special hot solder dip process on the piece parts prior to assembly. Another approach is to fully consume the tin plating by tin-lead solder during the SMT reflow process that occurs during circuit card assembly. This phenomenon of tin replacement during SMT reflow has been termed ''self-mitigation'', because the components mitigate themselves without the need of any special additional processing. Self-mitigation has many advantages over other forms of tin mitigation as it is highly effective, adds no additional cost and subjects the components to no additional handling.

The principal challenge to implementing self-mitigation as a standard practice is incomplete knowledge of the conditions under which components will reliably self-mitigate. Prior work concluded that for a specific set of process conditions, board finish, and pad design, self-mitigation can be predicted by the geometry of the component terminations [1]. It is not clear, however, how these results apply for other manufacturing processes, board finishes, and pad sizes. Without this understanding, the only reliable means for systems integrators to be confident that self-mitigation has been achieved on a given set of assemblies is to duplicate the conditions of the prior study or to perform direct measurements on the as-received hardware.

The existence of this knowledge gap prompted the Pb-free Electronics Risk Management Council (PERM, IPC Committee 8-81) to initiate a study in 2014 under IPC task group 8-81F. The first phase of that study has been completed and this report describes that study and the results to date.

Design of Experiment

Per the requirements of SAE GEIA-STD-0005-2, risk of tin whiskers is to be acceptably mitigated when there is 3% by weight of lead (Pb) alloyed with the tin. Therefore, the purpose of this study is to determine the conditions under which this level of alloying can be reliably achieved during SMT processing. (Since the alloys involved in the study are only binary tin lead alloys, a minimum of 3% Pb by weight is equivalent to a maximum of 97% Sn by weight.)

The task team decided to perform a new set of experiments involving the manufacture of identical sets of test vehicles at a number of different locations, all assembled to the requirements of IPC J-STD 001, Class 3. For simplicity, and to permit direct comparison with previous results, it was decided to use the same printed board layout and components from the initial 2010 study. Many potential factors for inclusion in the DOE were considered. The factors chosen for consideration are described in Table 1.

Table_1 Design of Experiment

Experimental Factor	Settings
Component Packages	16 different part numbers (details below)
Board finish	OSP and Sn Pb HASL
Pad size	Per initial study and 25% smaller
Manufacturing site	Seven different locations