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FOUNDRY PROCESS QUALIFICATION GUIDELINES – PRODUCT LEVEL

(Wafer Fabrication Manufacturing Sites)

JEP001-3A

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Contents

Foreword

The publication is divided into three parts, backend of line (JEP001-1A), transistor level (JEP001-2A), and product level testing (JEP001-3A). The document provides methodologies for the minimum set of measurements to qualify a new semiconductor wafer process. It is written with particular reference to a generic silicon based CMOS logic technology. While it may be applicable to other technologies (e.g., analog CMOS, bipolar, BICMOS, GaAs, etc.), some sections apply specifically to CMOS. No effort was made in the present document to cover all the qualification requirements for specific other technologies, e.g., Cu/Low K interconnects or ultra-thin gate oxide.

Any qualification requirements beyond the minimum set are to be developed for the specific performance expected of the technology. The minimum set of measurements and the requirements for the qualification based on those measurements are to be determined between the foundry and its customers on an individual basis The process technology owner (foundry) will be required to document the details of specific testing unique to the process being qualified.

The guideline documents common best practices in the semiconductor industry and updated in accordance to advancement in the semiconductor industry and JEDEC bylaws of periodic reviews.

Introduction

This publication, was originally published as JP-001 entitled 'Foundry Process Qualification Guidelines', it was co-sponsored by JEDEC and the FSA (Fabless Semiconductor Association). It originated at the FSA as a technology specific document, and has evolved into a generic set of qualification methodologies. The JEDEC sponsoring committee is JC-14 through its JC-14.2 subcommittee on wafer level reliability.

This document encompasses and references a number of other standards and procedures, some of which are in a state of constant revision and update. While a case might be made for producing a lean, concise guideline that does not spell out specific procedures or requirements, the proposition of spelling out the essence of a comprehensive set of methodologies in one place has a practical value that outweighs the case for simplicity.(comment : the requirements are only spelled out in a number of cases. Best to be consistent and let the existing JEDEC specs speak for themselves)

The three parts: JEP001-1A, JEP001-2A, and JEP001-3A are described below. It is intended that each part references the appropriate test and requirement noting that some tests may be performed on the package level. This standard should be read alongside reliability requirements established between the supplier and customer.

The structure of the JEDEC JEP001 series as currently conceived is as follows:

Part 1 – Backend of line testing
Part 2 – Transistor-level testing
Part 3 – Product-level testing

Acronyms

The following acronyms have been used in this document.

WLR: wafer level reliability
IMD: inter/intra-metal dielectric
HTOL: high temperature operating life
ESD: electrostatic discharge
HBM: human body model
MM: machine model
CDM: charged device model
TQV: technology qualification vehicle
PCM: process control monitor
FA: failure analysis

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(From JEDEC Board Ballot JCB-17-30, formulated under the co-sponsorship of the JC-14.2 Subcommittee on Wafer Level Reliability.)

1 Scope

This document describes package-level test and data methods for the qualification of semiconductor technologies. It does not give pass or fail values or recommend specific test equipment, test structures or test algorithms. Wherever possible, it references applicable JEDEC such as JESD47 or other widely accepted standards for requirements documentation.

There are two levels of qualification described. Level 1 is a pure process qualification intended to find reliability weaknesses. It primarily addresses technology wearout mechanisms through package or wafer level reliability tests on specially designed test structures.

Level 2 demonstrates the reliability of the process that corresponds to the reliability demands from projected or known applications. Level 2 testing can be implemented via the testing of a relevant functional technology qualification vehicle (TQV), including life test. The level 2 tests are described in clause 12. Other Reporting requirements (e.g., PCM data) are also included.

2 Quality system

It is the responsibility of the foundry to have the appropriate quality system in place with special emphasis on issues relating to equipment capability, maintenance and calibration, continuous improvement and process control. In particular, a functioning SPC methodology should be demonstrated for all key processes (see EIA/JEDEC EIA-557A). As a minimum the foundry will have ISO9001 certification. The ISO9001 audit results by a third party and subsequent corrective actions on deficiencies shall be made available to the customer upon request. For those supplying to automotive applications, the foundry may also have to demonstrate requirements from the IATF TS 16949 standard to meet the needs of these products.

3 Responsibilities

3.1 Level 1 qualification

The foundry is responsible for the design and implementation of the level 1 test vehicle (i.e., TESTCHIP). For the special case of a foundry customer driving process development, development of the level 1 test vehicle may be shouldered in whole or in part by the customer. The foundry shall fabricate the qualification silicon, execute the described level 1 tests and create the qualification report. The tests and qualification report may be done by the foundry or third party test vendor. The qualification requirements may be reduced for a derivative process, where the parent process has already been fully qualified at the same location.