JEDEC STANDARD

Board Level Cyclic Bend Test Method for Interconnect Reliability Characterization of SMT ICs for Handheld Electronic Products

JESD22-B113B

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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BOARD LEVEL CYCLIC BEND TEST METHOD FOR INTERCONNECT RELIABILITY CHARACTERIZATION OF SMT ICS FOR HANDHELD ELECTRONIC PRODUCTS

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Foreword

Printed circuit board assemblies experience various mechanical loading conditions during assembly and use. The repeated flexing (cyclic bending) of board during various assembly and test operations and in actual use can cause electrical failures due to circuit board and trace cracks, solder interconnects cracks, and the SMT IC cracks. Although the number of repeated bend cycles are small during assembly (e.g., handling between various assembly operations, In-circuit Testing, final assembly in product casing), the magnitude of flexure can be very significant. On the other hand, the actual use conditions such as repeated key-presses in mobile phone can result in a large number of repeated bend cycles during the life of the product, albeit at a lower magnitude.

Since SMT IC manufacturers and suppliers cannot evaluate their package performance on actual final products, a board level test method is needed to evaluate the performance of SMT ICs due to repeated bending of board and compare their performance with other SMT ICs.

This standard replaces JESD22-B113A, changes can be found in Annex B.

Introduction

The parameters specified in this test method were originally developed from the work performed by various members of JEDEC task group for board level cyclic bend test standardization. The task group was comprised of the following companies in alphabetical order:

Amkor Technology, Cisco Systems, Ericsson Mobile Platforms, Flextronics International, IBM Corporation, Infineon Technologies, Institute of Microelectronics, Intel Corporation, Nokia Mobile Phones, Research in Motion, SonyEricsson Mobile Communication, ST Microelectronics, Sun Microsystems, and Texas Instruments.

Please see Annex A to review the work conducted by the task group to develop special test boards and understand the effects of different test parameters.

BOARD LEVEL CYCLIC BEND TEST METHOD FOR INTERCONNECT RELIABILITY CHARACTERIZATION OF SMT ICS FOR HANDHELD ELECTRONIC PRODUCTS

(From JEDEC board Ballot, JCB-18-26, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

The Board Level Cyclic Bend Test Method is intended to evaluate and compare the performance of SMT ICs in an accelerated test environment for handheld electronic products applications. The purpose is to standardize the test methodology to provide a reproducible performance assessment of SMT ICs while duplicating the failure modes normally observed during product level test. This is not a SMT IC qualification test and is not meant to replace any product level test that may be needed to qualify a specific product and assembly.

Correlation between test and field conditions is not yet fully established. Consequently, the test procedure is presently more appropriate for relative SMT IC performance than for use as a pass/fail criterion. However, to do comparisons care must be taken to have the same test variables used, such as SMT IC configuration and size.

This standard assumes a surface mount device such as BGAs, LGAs (excluding sockets and connectors), TSOP, and CSPs. Discrete SMT devices, e.g., capacitors, resistors, etc., are outside the scope of this test method. Furthermore, this test method is only applicable for handheld products applications where cyclic bending due to repeated key-press operations is a concern. The size of surface mount device is limited to 15 mm x 15 mm maximum.

2 Apparatus

- Any cyclic bend test apparatus that can cause a repeated bending of printed wiring boards at 1 Hz to 3 Hz cyclic frequency for up to 200,000 cycles with maximum cross-head displacement of 4 mm. The cross-head displacement accuracy shall be +/- 5% of the maximum displacement.
- Strain monitoring equipment with minimum sample rate of at least 10 times the cyclic bending frequency with simultaneous sampling of all channels. The specific requirements for data recording are described in section 10.3. The strain monitoring equipment shall be as per IPC/JEDEC-9704 guidelines.
- Resistance monitoring equipment able to detect electrical failures as per the criteria defined in this standard. The sample rate of resistance monitoring equipment shall be at least 10 times the cyclic bending frequency with simultaneous sampling of all channels. In-Situ monitoring per IPC/JEDEC-9706 can be considered to provide instantaneous electrical monitoring.
- A system which monitors both PCB strain and electrical resistance of daisy chain nets at the same sampling rate is preferred, but not required.