

JEDEC STANDARD

Electrically Erasable Programmable ROM (EEPROM) Program / Erase Endurance and Data Retention Stress Test

JESD22-A117E

(Revision of JESD22-A117D, August 2018)

NOVEMBER 2018

JEDEC Solid State Technology Association



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2018
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2108

JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

**ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM / ERASE
ENDURANCE AND DATA RETENTION STRESS TEST**

CONTENTS

		Page
Foreword		ii
1	Scope	1
2	Terms and definitions	1
3	Apparatus	4
4	Procedure	4
	4.1 Program/erase endurance	6
	4.1.1 Test setup	6
	4.1.2 Data cycling	6
	4.2 Data retention	10
	4.2.1 Data programming	10
	4.2.2 Electrical testing and pattern verification	10
	4.2.3 Data retention stress	10
	4.2.4 Electrical testing and pattern verification	11
	4.3 Precautions	11
	4.4 Measurements	11
	4.4.1 Electrical measurements	11
	4.4.2 Required measurements	11
	4.4.3 Measurement conditions	11
5	Failure criteria	12
	5.1 Handling of transient failures	12
	5.2 Separation of failures into data errors and device failures	12
	5.3 Calculation of UBER	13
	5.3.1 Calculation of UBER in the ideal case	13
	5.3.2 Calculation of UBER in other cases	14
6	Summary	14
Annex A (informative) Differences between JESD22-A117D and its predecessors		15
A.1	(informative) Differences between JESD22-A117D and JESD22-A117C	15
A.2	(informative) Differences between JESD22-A117C and JESD22-A117B	15
A.3	(informative) Differences between JESD22-A117B and JESD22-A117A	16
A.4	(informative) Differences between JESD22-A117A and JESD22-A117	17