JEDEC
STANDARD

Low Power Double Data Rate 5 (LPDDR5)

JESD209-5

FEBRUARY 2019

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2019
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2108

JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

Contents

1 **Scope** 1
2 **Overview** 2
2.1 Features 2
2.2 Functional Description 2
2.2.1 Pad Definition and Description 2
2.2.2 Pin per byte 3
2.2.3 LPDDR5 Bank Architecture 4
2.2.3.1 Block diagram of bank configuration and Read operation outline 5
2.2.3.1.1 4 Bank / 4 Bank Groups Configuration 5
2.2.3.1.2 8 Bank Mode Configuration 6
2.2.3.1.3 16 Bank Mode Configuration 7
2.2.3.2 Address mapping 7
2.2.3.3 Bank architecture transition 7
2.2.3.4 Burst Operation 7
2.2.4 LPDDR5 SDRAM Addressing 13
2.2.5 Speed Grades 19
2.2.6 Burst Sequence 20
3 **WCK Clocking** 21
4 **Initialization and Training** 24
4.1 Power-up, Initialization and Power-off Procedure 24
4.1.1 Voltage Ramp and Device Initialization 24
4.1.2 Reset Initialization with Stable Power 28
4.1.3 Power-off Sequence 28
4.1.4 Uncontrolled Power-off Sequence 28
4.2 Training 29
4.2.1 ZQ Calibration 29
4.2.1.1 Calibration 29
4.2.1.1.1 Calibration During Powerup and Initialization 29
4.2.1.1.2 Background Calibration 29
4.2.1.1.3 Latching ZQ Calibration Results in Background Calibration Mode 30
4.2.1.1.4 Command-Based Calibration 31
4.2.1.1.5 Latching ZQ Calibration Results in Command-Based Calibration Mode 31
4.2.1.1.6 Maintaining Accurate Calibration - Background Calibration Mode 32
4.2.1.1.7 Maintaining Accurate Calibration - Command-Based Calibration Mode 32
4.2.1.1.8 Changing between Calibration Modes 33
4.2.1.1.8.1 Changing between Calibration Modes when DVFSQ is not active 33
4.2.1.1.8.2 Changing between Calibration Modes when DVFSQ is active 34
4.2.1.2 ZQ Stop Functionality 35
4.2.1.2.1 ZQ Resistor Sharing by Another Device(s) 35
4.2.1.2.1.1 ZQ Resistor Sharing in Background Calibration Mode 35
4.2.1.2.1.2 ZQ Resistor Sharing in Command-Based Calibration Mode 35
4.2.1.2.2 Stopping Background Calibration when DVFSQ is active 35
4.2.1.2.3 Stopping Background Calibration when VDDQ is Powered Off 36
4.2.1.3 ZQ Reset 37
4.2.1.4 Multi-die Package Considerations 38
4.2.1.4.1 Other Considerations in Background Calibration Mode 38
4.2.1.5 Other Considerations in Command-Based Calibration Mode 38
4.2.1.6 ZQ External Resistor, Tolerance, and Capacitive Loading 38

Contents (cont'd)

4.2.1.7 Flow Chart Examples 39
4.2.2 Command Bus Training 44
4.2.2.1 Command Bus Training Mode1 45
4.2.2.2 Command Bus Training Mode2 52
4.2.3 CA VREF Training....60
4.2.4 DQ VREF Training 60
4.2.5 WCK2CK Leveling 60
4.2.5.1 WCK2CK Leveling Mode (write-leveling called in LPDDR4) 60
4.2.5.2 WCK2CK Leveling Procedure and Related AC parameters 61
4.2.6 Duty Cycle Adjuster (DCA)....63
4.2.6.1 Duty Cycle Adjuster Range 63
4.2.6.2 The relationship between WCK waveform and DCA Code Change 64
4.2.6.3 The relationship between DCA Code Change and DQ output/RDQS timing 65
4.2.7 Duty Cycle Monitor (DCM) 66
4.2.7.1 DCM Functional Description....66
4.2.7.2 DCM Sequence 66
4.2.8 READ DQ Calibration....68
4.2.8.1 READ DQ Calibration Training Procedure....68
4.2.8.2 READ DQ Calibration Example 70
4.2.8.3 READ DQ Calibration after Power Down Exit 71
4.2.9 WCK-DQ Training....72
4.2.9.1 Training procedure....72
4.2.9.2 WCK-RDQS_t/Parity Training....73
4.2.9.3 FIFO Pointer Reset and Synchronism 74
4.2.9.4 Command constraints for Write/Read FIFO command....79
4.2.10 RDQS toggle mode....81
4.2.11 Enhanced RDQS training mode....82
5 Simplified LPDDR5 State Diagram 85
6 Mode Register Definition....90
6.1 Mode Register Assignment and Definition in LPDDR5 SDRAM 90
6.2 Mode Register Definition 93
6.2.1 Mode Register definition....93
7 Operating 137
7.1 Truth Table....137
7.1.1 Command Truth Table 137
7.2 WCK Operation 140
7.2.1 WCK2CK Synchronization operation....140
7.2.1.1 WCK2CK Synchronization 140
7.2.1.2 CAS Command with WCK2CK Synchronization Bits 140
7.2.1.3 WCK2CK Sync operation followed by a WRITE command....141
7.2.1.4 WCK2CK Sync operation followed by a READ command 143
7.2.1.5 WCK2CK Sync operation with CAS(WS_FAST=1)....146
7.2.1.6 Rank to rank WCK2CK Sync operation....148
7.2.2 WCK2CK SYNC Off Timing Definition 149
7.2.3 Write Clock Free Running mode....159
7.3 Row operation....162
7.3.1 Active Command 162
7.3.1.1 8 Bank mode SDRAM Operation 164
7.3.1.2 BG mode SDRAM Operation....164

Contents (cont'd)

7.3.2 Pre-Charge Operation 165
7.3.2.1 Pre-Charge Operation 165
7.3.2.2 Auto-Precharge Operation 169
7.3.2.2.1 Delay time from Write to Read with Auto Precharge 170
7.3.2.2.2 Burst Read with Auto-Precharge 171
7.3.2.2.3 Burst Write with Auto-Precharge 172
7.4 Read/Write Operation 174
7.4.1 Read and Write Access Operations 174
7.4.2 Read Preamble and Postamble 174
7.4.3 Burst Read Operation 174
7.4.3.1 Read Timing 174
7.4.3.2 Read to Read Operation without additional WCK2CK-sync 176
7.4.3.3 Read to Read Operation with additional WCK2CK-sync 177
7.4.3.4 Read operation followed by write operation 177
7.4.4 READ Burst end to PRECHARGE Delay (tRBTP) 178
7.4.5 RDQS Mode 179
7.4.5.1 RDQS Timing 179
7.4.5.2 RDQS Related Functionalities 180
7.4.5.3 Mode Registers for RDQS 181
7.4.5.4 RDQS Pattern Definition 182
7.4.6 Write Preamble and Postamble 185
7.4.7 Burst Write Operation 185
7.4.7.1 Write Timing 185
7.4.7.2 Write to Write Operation without additional WCK2CK-sync 187
7.4.7.3 Write to Write Operation with additional WCK2CK-sync 188
7.4.7.4 Write operation followed by read operation 188
7.4.8 Read and Write Latency 189
7.4.8.1 Read and Read-to-Precharge Latencies 189
7.4.8.2 Write Latency 190
7.4.8.3 Write Recovery time 193
7.4.9 Masked Write 195
7.4.10 Data Mask (DM) and Data Bus Inversion (DBI-DC) Function 200
7.4.10.1 DMI Pin Behavior with Write Related Commands 201
7.4.10.2 DMI Pin Behavior with Read Related Commands 203
7.5 Refresh operation 204
7.5.1 Refresh command 204
7.5.2 Refresh Requirement 211
7.5.3 Self Refresh Operation 212
7.5.3.1 Power Down Entry and Exit during Self refresh 214
7.5.3.2 Command input Timing after Power Down Exit during Self Refresh 216
7.5.3.3 Self Refresh AC Timing Table 217
7.5.3.4 MRR, MRW, RFF, WFF, RDC, MPC Command during tXSR 218
7.5.4 Partial Array Self Refresh (PASR) 219
7.5.4.1 PASR Segment Masking 219
7.5.5 Power Down 220
7.5.6 Power-Down Entry and Exit 220
7.5.7 Sleep Mode 226
7.6 Other Operation 228
7.6.1 Mode Register Read 228

Contents (cont’d)

7.6.1.1 MRR after Read and Write Command 230
7.6.1.2 MRR after Power-Down Exit....232
7.6.2 Mode Register Write 233
7.6.2.1 Mode Register Write Disable control for Byte Mode device 233
7.6.3 Frequency Set Point....234
7.6.3.1 Frequency set point update Timing 235
7.6.3.2 Frequency set point update Timing for DVFSC and DVFSQ 236
7.6.4 On-Die Termination (ODT) 239
7.6.4.1 On-Die Termination for Command/Address Bus....239
7.6.4.1.1 ODT Mode Register and ODT State Table for Command/Address Bus 239
7.6.4.1.2 ODT Mode Register and ODT Characteristics for Command/Address Bus....241
7.6.4.1.3 ODT update time for Command/Address Bus....242
7.6.4.2 On-Die Termination for Data Bus 243
7.6.4.2.1 ODT Mode Register for Data Bus 243
7.6.4.2.2 Asynchronous ODT for Data Bus 243
7.6.4.2.3 ODT Mode Register and ODT Characteristics for Data Bus....245
7.6.4.3 On-Die Termination for WCK_t and WCK_c 247
7.6.4.3.1 ODT Mode Register for WCK_t/c 247
7.6.4.3.2 ODT during WCK2CK training 247
7.6.5 Non-target ODT....248
7.6.5.1 Non-target DRAM ODT control 249
7.6.5.2 Asynchronous NT-ODT 252
7.6.5.3 Timing diagram of Write case 256
7.6.5.4 Timing diagram of Read case....257
7.6.6 Input Clock Stop and Frequency Change....257
7.6.7 V_{REF} Current Generator (VRCG) 258
7.6.8 Thermal Offset 259
7.6.9 Temperature Sensor....259
7.6.10 Multi-Purpose Command (MPC) 261
7.6.11 tWCK2DQ Interval Oscillator....261
7.6.11.1 Interval Oscillator Matching Error....264
7.7 Specific features, Reliability & Power-optimization 265
7.7.1 Dynamic Voltage and Frequency Scaling (DVFS) 265
7.7.1.1 DVFSC Mode....265
7.7.1.2 DVFSQ Mode....267
7.7.1.2.1 DVFSQ High-to-Low Transition....268
7.7.1.2.2 DVFSQ Low-to-High Transition without VRCG during VDDQ ramp 269
7.7.1.2.3 DVFSQ Low-to-High Transition with VRCG....270
7.7.2 Data Copy Low Power Function....271
7.7.2.1 Write Data Copy Function....271
7.7.2.2 Read Data Copy Function....273
7.7.2.3 Read Data Copy Function with Read DBI Enable 274
7.7.3 Write X operation....274
7.7.4 Post Package Repair (PPR)....278
7.7.4.1 Guard Key Protection....279
7.7.4.2 PPR Fail Row Address Repair....280
7.7.5 Target Row Refresh 281
7.7.5.1 TRR Mode Operation 282
7.7.6 Decision Feedback Equalization (DFE)....283

Contents (cont'd)

7.7.7 Link ECC 284
7.7.8 Single-ended mode for Clock, Write Clock and RDQS 291
7.7.8.1 Restriction of Single-ended mode 292
7.7.8.2 Switching sequence between Single-ended and Differential 293
7.7.8.3 VRCG Enable timing 294
7.7.8.4 AC parameters for Single Ended (SE) 295
7.7.8.5 Command bus training procedure 295
8 Command Constraint and AC timing 296
8.1 Effective Burst Length (BL/n) Definition 296
8.1.1 Auto Precharge Command Timing Constraints 304
8.1.2 CAS Command Timing Constraints 308
8.1.3 Training related timing constraints 317
8.1.4 MRR/MRW Timing Constraints 318
8.1.5 Rank to Rank Command Timing Constraints 320
9 AC Timing 323
9.1 Core AC Timing Parameters by Speed Grade 323
9.1.1 Timing table for x16, DVFSC Disabled & Link ECC Disabled 323
9.1.1.1 Timing Table for x8 (Byte Mode) SDRAM 324
9.1.1.2 Timing Table for Link ECC is enabled 325
9.1.1.3 Timing Table for x8 (Byte Mode) SDRAM and Link ECC is enabled 326
9.1.2 Timing table for x16, DVFSC Enabled & Link ECC Disabled 327
9.1.2.1 Timing Table for x8 (Byte Mode) SDRAM 327
9.2 Core AC Temperature derating for AC Timing 328
10 Absolute Maximum DC Ratings 329
11 AC and DC Operating Condition 330
11.1 Recommended DC Operating Conditions 330
11.2 Input Leakage Current 332
11.3 Input/Output Leakage Current 332
11.4 Operating Temperature Range 332
11.4.1 Operating Temperature Range (Automotive spec addendum only) 333
11.5 Electrostatic Discharge Sensitivity Characteristics 333
12 AC and DC Input/Output Measurement levels 334
12.1 1.05V High speed LVCMOS 334
12.1.1 Standard specifications 334
12.1.2 Input Level for Reset_n 334
12.1.3 Input Level for CS 334
12.1.4 AC Overshoot / Undershoot 334
12.1.4.1 AC Overshoot / Undershoot 334
12.1.4.2 AC Overshoot / Undershoot for LVSTL 334
12.2 Differential Input Voltage 335
12.2.1 Differential Input Voltage for CK 335
12.2.1.1 Peak Voltage Calculation Method 336
12.2.1.2 Single ended Input Voltage for CK 337
12.2.1.3 Differential Input Slew Rate Definition for CK 338
12.2.1.4 Differential Input Cross Point Voltage for CK 339
12.2.2 Differential Input Voltage for WCK 340
12.2.2.1 Peak Voltage Calculation Method 341
12.2.2.2 Single ended Input Voltage for WCK 342
12.2.2.3 Differential Input Slew Rate Definition for WCK 343

Contents (cont'd)

12.2.2.4 Differential Input Cross Point Voltage for WCK 344
12.3 Output Slew Rate 345
12.3.1 Single Ended Output Slew Rate....345
12.3.2 Differential Output Slew Rate 346
12.4 Driver Output Timing Reference load....346
12.5 Single Ended WCK 347
12.5.1 Single Ended WCK input definitions 347
12.5.2 Single Ended Mode WCK Pulse Definitions 347
12.6 Single Ended CK 348
12.6.1 Single Ended CK input definitions 348
12.6.2 Single Ended Mode CK Pulse Definitions....349
12.7 Read Timing tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation 350
12.7.1 tLZ(RDQS) tLZ(DQ) tHZ(RDQS) tHZ(DQ)....350
12.7.1.1 tLZ(RDQS) and tHZ(RDQS) Calculation for ATE(Automatic Test Equipment) 350
12.7.1.2 tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment) 352
13 Input / Output Capacitance....355
14 IDD Specification Parameters and Test Conditions 356
14.1 IDD Measurement Conditions....356
14.2 IDD Specifications 366
15 Electrical Characteristics and AC Timing 370
15.1 Clock Specification....370
15.1.1 Definition for tCK(avg) and nCK....370
15.1.2 Definition for tCK(abs) 370
15.1.3 Definition for tCH(avg) and tCL(avg) 370
15.1.4 Definition for tCH(abs) and tCL(abs) 371
15.1.5 Definition for tJIT(per)....371
15.1.6 Definition for tJIT(cc) 371
15.1.7 Clock Timing 371
15.2 Write Clock Specification 373
15.2.1 Definition for tWCK(avg) and nWCK....373
15.2.2 Definition for tWCK(abs) 373
15.2.3 Definition for tWCH(avg) and tWCL(avg) 373
15.2.4 Definition for tWCH(abs) and tWCL(abs) 374
15.2.5 Definition for tJIT(per)....374
15.2.6 Definition for tJIT(cc) 374
15.2.7 Definition for tERR(2per)....374
15.2.8 Definition for tERR(3per)....374
15.2.9 Definition for tERR(4per)....375
15.2.10 Write Clock Timing 375
15.3 tWCK2DQ AC parameters 377
15.4 DQ Tx Jitter Spec 377
15.5 CS Rx specification....380
15.5.1 CS Rx mask and single pulse definition for Synchronous mode 380
15.5.2 CS Rx input level definition for Asynchronous mode....381
15.5.3 Synchronous mode CS Rx mask / single pulse spec and Asynchronous mode CS input ... 382
15.6 CA Rx specification 383
15.6.1 CA Rx mask and single pulse definition 383
15.6.2 CA Rx mask and single pulse spec. 385
15.7 DQ, DMI, Parity and DBI Rx specification 386

Contents (cont'd)

15.7.1 DQ, DMI, Parity and DBI Rx mask and single pulse definition..386
15.7.2 DQ, DMI, Parity and DBI Rx mask and single pulse spec. 389
15.8 Pull Up/Pull Down Driver Characteristics and Calibration 390
15.9 Output Driver and Termination Resistance Temperature and Voltage Sensitivity 391
16 Die configuration, Package ballout & Pin Definition 393
16.1 Package Configuration 393
16.1.1 Package Considerations for Byte-Mode Devices..393
16.2 Pad Order...394
16.3 Package Ballout 395
16.4 Package Die Layout..395
16.5 Package Configuration 395
16.6 ZQ Wiring 396

Figures

Figure 1 — BG Mode Configuration Example (One Channel Shown)...5
Figure 2 — 8B Mode Configuration Example (One Channel Shown) 6
Figure 3— 16B Mode Configuration Example (One Channel Shown) 7
Figure 4 — Read Operation BG mode, CKR (WCK vs. CK) = 4:1, BL=16...8
Figure 5 — Read Operation BG mode, CKR (WCK vs. CK) = 4:1, BL=32...9
Figure 6 — Read Operation 8B mode, CKR (WCK vs. CK) = 4:1, BL=32 10
Figure 7 — Read Operation 16B mode, CKR (WCK vs. CK) = 4:1, BL=16 11
Figure 8 — Read Operation 16B mode, CKR (WCK vs. CK) = 4:1, BL=32 12
Figure 9 — Clocking and Interface Relationship 21
Figure 10 — Block Diagram of an example system...22
Figure 11 — DRAM internal WCK2CK auto-sync process...23
Figure 12 — Requirement for Voltage Ramp Control...25
Figure 13 — Power Ramp and Initialization Sequence 26
Figure 14 — Background ZQ Calibration Timing..30
Figure 15 — Background to Command-based Switching when DVFSQ is not active...............................33
Figure 16 — Command-based to Background Switching when DVFSQ is not active 33
Figure 17 — Background to Command-based Switching when DVFSQ is active......................................34
Figure 18 — Command-based to Background Switching when DVFSQ is active......................................34
Figure 19 — ZQCal Timing 37
Figure 20 — Initialization to Background Calibration Flow Chart, no DVFSQ support...............................39
Figure 21 — Initialization to Command-based Calibration Flow Chart, no DVFSQ support, option 1 (check Master) 40
Figure 22 — Initialization to Command-based Calibration Flow Chart, no DVFSQ support, option 2 (ignore Master)...41
Figure 23 — Initialization to Background Calibration Flow Chart, with DVFSQ support 42
Figure 24 — Initialization to Command-based Calibration Flow Chart, with DVFSQ support....................43
Figure 25 — Entering Command Bus Training Mode and CA Training Pattern Input and Output (WCK Frequency change) 48
Figure 26 — Entering Command Bus Training Mode and CA Training Pattern Input and Output (Fixed WCK Frequency) 49
Figure 27 — Exiting Command Bus Training Mode 50
Figure 28 — Entering Command Bus Training Mode and CA Training Pattern Input with VREF(CA) Value Update (WCK Frequency change) 55
Figure 29 — Entering Command Bus Training Mode and CA Training Pattern Input with VREF(CA) Value Update (Fixed WCK Frequency) 56
Figure 30 — CA pattern Input/Output to Vref setting Input..57
Figure 31 — Consecutive CA training pattern Input/Output 57
Figure 32 — Exiting Command Bus Training Mode 58

Contents (cont'd)

Figure 33 — WCK2CK Leveling Entry 61
Figure 34 — WCK2CK Leveling Exit 61
Figure 35 — Relationship between WCK waveform and DCA Code Change (Example) 64
Figure 36 — Relationship between WCK waveform and DQS_t/c and DQ output (Example) 65
Figure 37 — DCM timing example 67
Figure 38 — Read DQ Calibration Timing: Read to Read DQ Calibration 69
Figure 39 — Read DQ Calibration Timing: Read DQ Calibration to Read DQ Calibration 70
Figure 40 — READ DQ CALIBRATION following Power Down State 71
Figure 41 — Consecutive Write FIFO Operation timing for BG mode: CKR (WCK vs. CK) = 4:1 75
Figure 42 — Consecutive Read FIFO Operation timing for BG mode: CKR (WCK vs. CK) = 4:1 76
Figure 43 — Consecutive Write FIFO Operation timing: Parity Data input for BG mode: CKR (WCK vs. CK) = 4:1 77
Figure 44 — Consecutive Read FIFO Operation timing: Parity Data output for BG mode: CKR (WCK vs. CK) = 4:1 78
Figure 45 — Write FIFO to Read FIFO Timing for BG mode: CKR (WCK vs. CK) = 4:1 79
Figure 46 — Read FIFO to Write FIFO Timing for BG mode: CKR (WCK vs. CK) = 4:1 80
Figure 47 — RDQS toggle mode entry timing example 81
Figure 48 — RDQS toggle mode exit timing example 82
Figure 49 — Enhanced RDQS training mode entry timing 83
Figure 50 — Enhanced RDQS training mode exit timing 83
Figure 51 — Read operation during Enhanced RDQS training mode 84
Figure 52 — LPDDR5: Simplified Bus Interface State Diagram 86
Figure 53 — Sub-State Diagram-1 related with MRR, MRW, CAS, WFF, RFF, RDC and MPC Command 87
Figure 54 — Sub-State Diagram-2: related with MPC State 88
Figure 55 — Aligned WCK/2_0 to CK (Left) & Miss-Aligned WCK/2_0 to CK (Right) 140
Figure 56 — LPDDR5 WCK2CK Sync operation by CAS command with WCK2CK Sync operand enabled 141
Figure 57 — WCK2CK Sync operation followed by a WRITE command 142
Figure 58 — WCK2CK Sync operation followed by a READ command 143
Figure 59 — Minimum latency WCK2CK Sync operation for CAS(WS_FAST=1) 146
Figure 60 — WCK2CK sync operation for Read Operation with CAS(WS_FAST=1) with command gap 146
Figure 61 — Minimum gap rank to rank read operation with WCK2CK Sync after completing DQ burst in one rank 148
Figure 62 — Simultaneous WCK2CK Sync process for multi-ranks (especially two ranks) 148
Figure 63 — Write sync off timing BG Mode, CKR (WCK vs. CK) = 4:1, BL=16 154
Figure 64 — Write sync off timing (WCK2CK Sync is expired), BG Mode, CKR (WCK vs. CK) = 4:1, BL=16 154
Figure 65 — Write sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=32 155
Figure 66 — Masked Write sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=16 155
Figure 67 — Read sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=16, tRPST=2.5nWCK 156
Figure 68 — Read sync off timing (WCK2CK Sync is expired) BG Mode, CKR = 4:1, BL=16, tRPST=2.5nWCK 156
Figure 69 — Read sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=16, tRPST=4.5nWCK 157
Figure 70 — Read sync off timing (WCK2CK Sync is expired) BG Mode, CKR = 4:1, BL=16, tRPST=4.5nWCK 157
Figure 71 — Read sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=32, tRPST=2.5nWCK 158
Figure 72 — Read sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=32, tRPST=4.5nWCK 158
Figure 73 — WCK free running mode starting with WCK2CK-sync operation followed by a write command 160
Figure 74 — Figure 2. WCK free running mode starting with WCK2CK-sync operation followed by a read command 160

Contents (cont’d)

Figure 75 — CAS Command based WCK Buffer off following write command min(tWCKOFF) = RU(max(tWCKDQO)/tCK) + BL/n + 1, where n=8 in WCK:CK=4:1 mode and n=4 in WCK:CK=2:1 mode 161
Figure 76 — CAS Command based WCK Buffer off following read command min(tWCKOFF) = RU(max(tWCKDQO)/tCK) + BL/n + 1, where n=8 in WCK:CK=4:1 mode and n=4 in WCK:CK=2:1 mode 161
Figure 77 — Activate command for 8B/16B mode 162
Figure 78 — Activate Command with Activate1 and Activate-2 spacing for 8B/16B mode 163
Figure 79 — Activate command for BG mode 163
Figure 80 — 8 Bank tFAW Timing 164
Figure 81 — BG mode tFAW timing 164
Figure 82 — Burst Read followed by Precharge: 16B Mode, CKR = 4:1, BL=16 167
Figure 83 — Burst Read followed by Precharge: 16B Mode, CKR = 4:1, BL=32 168
Figure 84 — Burst Write Followed by Precharge: 16B Mode, CKR = 4:1, BL=16 169
Figure 85 — Command Input Timing with RAS lock 170
Figure 86 — Delay time from Write to Read with Auto Precharge: 16B mode 170
Figure 87 — Burst Read with Auto-Precharge: 16B mode 171
Figure 88 — Burst Write with Auto- Precharge: 16B mode 172
Figure 89 — Burst Read Operation 175
Figure 90 — Back to back read operation with tCCD(min) = 2tCK 176
Figure 91 — Back to back read operation with tCCD ≤ RL + BL/n 176
Figure 92 — Back to back read operation requiring a new WCK2CK-sync sequence 177
Figure 93 — Read operation followed by write operation without additional WCK2CK-sync sequence 177
Figure 94 — Read operation followed by write operation with additional WCK2CK-sync sequence 177
Figure 95 — Example of READ burst end to PRECHARGE command delay for same banks 178
Figure 96 — Example of READ burst end to PRECHARGE command delay for same banks 178
Figure 97 — Example of READ burst end to PRECHARGE command delay for same banks 178
Figure 98 — Example of READ burst end to PRECHARGE command delay for same banks 179
Figure 99 — Read timing with RDQS and related timing parameters 180
Figure 100 — 4 All the possible types of RDQS 181
Figure 101 — READ16 to READ16 2nCK Gap Operation: CKR (WCK vs. CK) = 4:1, tRPST=2.5nWCK 182
Figure 102 — BG Mode Read32 Operation: CKR (WCK vs. CK) = 4:1, tRPST=2.5nWCK 182
Figure 103 — Burst Write Operation 186
Figure 104 — Back to back write operation with tCCD(min) = 2tCK 187
Figure 105 — Back to back write operation with tCCD ? WL + BL/n (n=4 at WCK:CLK=2:1, n=8 at WCK:CLK=4:1) 187
Figure 106 — Back to back write operation requiring a new WCK2CK-sync sequence 188
Figure 107 — Write operation followed by read operation 188
Figure 108 — Write Latency Timing 192
Figure 109 — Write Recovery Latency Timing 194
Figure 110 — Masked Write Command – Same Bank Operation Timing without any other DQ operation commands in 4 Bank/4BG or 16 Bank mode 196
Figure 111 — Masked Write Command – Different Bank Group Operation Timing in 4 Bank/4BG mode 197
Figure 112 — Masked Write Command – Different Bank Operation Timing in 8 Bank Mode (BL32 only) 198
Figure 113 — Masked Write Command – 16 Bank Mode (WCK:CK = 2:1) 199
Figure 114 — All-Bank Refresh Operation 208
Figure 115 — Per-Bank Refresh Operation 208
Figure 116 — Postponing Refresh Commands (Example) 210
Figure 117 — Pulling-in Refresh Commands (Example) 211
Figure 118 — Self Refresh Entry/Exit Timing 213
Figure 119 — Self Refresh Entry/Exit Timing with Power Down Entry/Exit 214

Contents (cont’d)

Figure 120 — Self Refresh Entry with PD=”1” Timing 215
Figure 121 — Command input timing after Power Down Exit during Self Refresh 216
Figure 122 — MRR, MRW, WFF, RFF, RDC and MPC Commands Issuing Timing during tXSR 218
Figure 123 — Basic Power-Down Entry and Exit Timing 221
Figure 124 — Read and Read with Auto Precharge to Power-Down Entry 221
Figure 125 — Write and Mask Write to Power-Down Entry 222
Figure 126 — Write with Auto Precharge and Mask Write with Auto Precharge to Power-Down Entry .. 222
Figure 127 — Refresh Entry to Power-Down Entry 223
Figure 128 — Self Refresh Entry/Exit Timing with Power Down Entry/Exit 223
Figure 129 — Activate Command to Power-Down Entry 223
Figure 130 — Precharge Command to Power-Down Entry 224
Figure 131 — Mode Register Read to Power-Down Entry 224
Figure 132 — Mode Register Write to Power-Down Entry 224
Figure 133 — Multi Purpose Command for Start ZQ Calibration to Power-Down Entry 225
Figure 134 — Deep Sleep Mode state diagram 226
Figure 135 — Deep Sleep Mode Entry in IDLE state and Exit Timing 227
Figure 136 — Deep Sleep Mode Entry in Self Refresh state and Exit Timing 227
Figure 137 — Mode Register Read Operation 229
Figure 138 — READ to MRR Timing 230
Figure 139 — WRITE to MRR Timing 231
Figure 140 — MRR Following Power-Down 232
Figure 141 — Mode Register Write Timing 233
Figure 142 — Frequency Set Point Switching Timing 235
Figure 143 — Training Three Frequency Set-Points 237
Figure 144 — Switching Between Two Trained Frequency Set-Points (Example) 238
Figure 145 — Switching to a Third Trained Frequency Set-Point (Example) 238
Figure 146 — Functional Representation of Command/Address bus ODT 239
Figure 147 — On Die Termination for Command/Address Bus 241
Figure 148 — ODT for Command/Address setting update timing 242
Figure 149 — Functional Representation of Data bus ODT 243
Figure 150 — Asynchronous ODTon/ODToff Timing 245
Figure 151 — On Die Termination for Data Bus 245
Figure 152 — Functional Representation of WCK ODT 247
Figure 153 — DRAM ODT configuration of Non-target DRAM ODT mode 248
Figure 154 — ODT Control on Non-target DRAM for Write 256
Figure 155 — ODT Control on Non-target DRAM for Read 257
Figure 156 — VRCG Enable Timing 258
Figure 157 — VRCG Disable Timing 258
Figure 158 — Temp Sensor Timing 260
Figure 159 — Interval oscillator offset 264
Figure 160 — DVFSC High (VDD2H) to Low (VDD2L) Transition 265
Figure 161 — DVFSC Low (VDD2L) to High (VDD2H) Transition 266
Figure 162 — Example DVFSC Block Diagram 266
Figure 163 — DVFSQ High (VDDQ) to Low Transition Flow Chart 268
Figure 164 — DVFSQ High (VDDQ) to Low Transition Timing 268
Figure 165 — DVFSQ Low (VDDQ) to High (VDDQ) Transition Flow Chart without VRCG 269
Figure 166 — DVFSQ Low (VDDQ) to High Transition Timing without VRCG during VDDQ ramp 269
Figure 167 — DVFSQ Low (VDDQ) to High (VDDQ) Transition Flow Chart with VRCG 270
Figure 168 — DVFSQ Low (VDDQ) to High Transition with VRCG 270
Figure 169 — Data copy granularity and reference data configuration in BL32 271
Figure 170 — Example of Write Data Copy Function Timing Diagram 273
Figure 171 — Example of Read Data Copy Function Timing Diagram 274
Figure 172 — Write X timing at Sync off: BG Mode, CKR (WCK vs. CK) = 4:1, BL=16 275

Contents (cont'd)

Figure 173 — Consecutive Write and Write X timing at Sync off: BG Mode, CKR (WCK vs. CK) = 4:1, BL=16 276
Figure 174 — Consecutive Write and Write X timing at Sync: BG Mode, CKR (WCK vs. CK) = 4:1, BL=16 276
Figure 175 — Write w/ write X issuing timing at Sync state. 277
Figure 176 — CAS_WRX Command timing after WCK2CK sync state is expired 277
Figure 177 — Guard Key Timing Diagram 279
Figure 178 — PPR Timing 280
Figure 179 — Target Row Refresh Mode 283
Figure 180 — DFE pre-drive requirement 284
Figure 181 — Write command showing link ECC transfer 285
Figure 182 — Read command showing Link ECC transfer 285
Figure 183 — Data flow on a memory Write operation 289
Figure 184 — Data flow on a memory Read operation 290
Figure 185 — SE to Differential CK and Write DQS -FSP Switching Timing 293
Figure 186 — Differential to SE CK and Write DQS -FSP Switching Timing 293
Figure 187 — VRCG status change to high current mode: Single-ended Clock Case 294
Figure 188 — VRCG status change to high current mode: Differential Clock Case 294
Figure 189 — Write Timing Diagram (BG mode, CKR=4:1, BL32) Example for BL/n, BL/n_min and BL/n_max 297
Figure 190 — DC Voltage Range 331
Figure 191 — VDDQ Tolerance Definition in Allowable Range 331
Figure 192 — Zprofile/Z(f) of the system at the DRAM package solder ball (without DRAM component) 331
Figure 193 — Overshoot and Undershoot Definition 335
Figure 194 — CK Differential Input Voltage 335
Figure 195 — Definition of differential Clock Peak Voltage 336
Figure 196 — Clock Single ended Input Voltage 337
Figure 197 — Differential Input Slew Rate Definition for CK_t, CK_c 338
Figure 198 — Differential Input Slew Rate Definition for CK_t, CK_c 339
Figure 199 — WCK Differential Input Voltage 340
Figure 200 — Definition of differential WCK Peak Voltage 341
Figure 201 — WCK Single ended Input Voltage 342
Figure 202 — Differential Input Slew Rate Definition for WCK_t, WCK_c 343
Figure 203 — Vix Definition (WCK) 344
Figure 204 — Single Ended Output Slew Rate Definition 345
Figure 205 — Differential Output Slew Rate Definition 346
Figure 206 — Driver Output Reference Load for Timing and Slew Rate 346
Figure 207 — Single Ended Mode WCK input Voltage 347
Figure 208 — Single Ended Mode WCK pulse 347
Figure 209 — Single Ended Mode CK input Voltage 348
Figure 210 — Single Ended Mode CK pulse 349
Figure 211 — tLZ(RDQS) method for calculating transitions and end point 350
Figure 212 — tHZ(RDQS) method for calculating transitions and end point 351
Figure 213 — tLZ(DQ) method for calculating transitions and end point 352
Figure 214 — tHZ(DQ) method for calculating transitions and end point 353
Figure 215 — DQ to RDQS 0UI read data timing example 377
Figure 216 — DQ to RDQS 3UI read data timing example 377
Figure 217 — Read burst example for pin DQx depicting bits 0 and 5 relative to the RDQS edge for 0 UI mismatch 378
Figure 218 — Read burst example for pin DQx depicting bits 0 and 5 relative to the RDQS edge for 3UI mismatch 378
Figure 219 — Synchronous mode CS Rx Mask definition 380
Figure 220 — Synchronous mode CS Rx single pulse definition 380

Contents (cont'd)

Figure 221 — Synchronous mode CS Timings at the DRAM Pin....381
Figure 222 — Asynchronous mode ViHPD and ViLPD at Power Down Exit....381
Figure 223 — CA Rx Mask definition....383
Figure 224 — CA Rx single pulse definition....383
Figure 225 — CA timings at the DRAM Pins....384
Figure 226 — DQ, DMI, Parity and DBI Rx Mask definition....386
Figure 227 — DQ to WCK tWCK2DQI and tDQ2DQ Timings at the DRAM pins referenced from the internal latch....387
Figure 228 — DQ, DMI, Parity and DBI Rx single pulse definition....388
Figure 229 — Example of rank assignment for a single-channel dual-rank package....393

Tables

Table 1 — Pad Definition and Description....2
Table 2 — Pins Per-Byte Signal List/Description for Link Protection disabled....3
Table 3 — Pins Per-Byte Signal List/Description for Link Protection enabled....3
Table 4 — Address Array mapping....7
Table 5 — LPDDR5 SDRAM x16 mode Addressing for BG Mode (4Banks/4Bank Groups)....13
Table 6 — LPDDR5 SDRAM x8 mode Addressing for BG Mode....14
Table 7 — LPDDR5 SDRAM x16 mode Addressing for 8B Mode....15
Table 8 — LPDDR5 SDRAM x8 mode Addressing for 8B Mode....16
Table 9 — LPDDR5 SDRAM x16 mode Addressing for 16B Mode....17
Table 10 — LPDDR5 SDRAM x8 mode Addressing for 16B Mode....18
Table 11 — LPDDR5 Speed Grades....19
Table 12 — Burst Sequence for READ (8 bank mode)....20
Table 13 — Burst Sequence for READ (4 bank/ 4Bank Group mode or 16Bank mode)....20
Table 14 — Burst sequence for Write....20
Table 15 — Example Clock and Interface Signal Frequency Relationship....22
Table 16 — MRS Default setting....24
Table 17 — Voltage Ramp Conditions....24
Table 18 — Initialization Timing Parameters....27
Table 19 — Reset Timing Parameter....28
Table 20 — Power Supply Conditions....28
Table 21 — Power Supply Conditions....28
Table 22 — ZQ Calibration Timing Parameters....36
Table 23 — Mapping of CA Input pin and DQ Output pin....45
Table 24 — Command Bus Training Mode1 AC Timing Table....51
Table 25 — Mapping of MR12 OP Code and DQ Numbers....53
Table 26 — Mapping of CA Input pin and DQ Output pin....53
Table 27 — Command Bus Training Mode2 AC Timing Table....59
Table 28 — WCK2CK Leveling Timing Parameters....62
Table 29 — DCA Range....63
Table 30 — Duty Cycle Adjuster Range....63
Table 31 — Duty cycle monitor timing....67
Table 32 — Invert Mask or output data fix0 Assignments in X16 Mode....69
Table 33 — Invert Mask or output data fix0 Assignments in X8 Mode....69
Table 34 — Read DQ Calibration Bit Ordering, Inversion, output data fix0 example for DQ....70
Table 35 — Read DQ Calibration Bit Ordering, Inversion, output data fix0 example for DMI....71
Table 36 — Enhanced RQDS training mode entry and exit timings....84
Table 37 — Mode Register Assignment in LPDDR5 SDRAM....90
Table 38 — MR0 Register Information (MA [7:0] = 00_H)....93
Table 39 — MR0 definition....93
Table 40 — MR1 Register Information (MA[5:0] = 01_H)....94
Table 41 — MR1 definition....94

Contents (cont'd)

Table 42 — MR2 Register Information (MA[7:0] = 02_H) 96
Table 43 — MR2 Definition 96
Table 44 — MR3 Register Information (MA[7:0] = 03_H) 98
Table 45 — MR3 Definition 98
Table 46 — MR4 Register Information (MA[7:0] = 04_H) 99
Table 47 — MR4 Definition 99
Table 48 — MR5 Register Information (MA[7:0] = 05_H) 100
Table 49 — MR5 Definition 100
Table 50 — MR6 Register Information (MA[7:0] = 06_H) 100
Table 51 — MR6 Definition 100
Table 52 — MR7 Register Information (MA[7:0] = 07_H) 100
Table 53 — MR7 Definition 100
Table 54 — MR8 Register Information (MA[7:0] = 08_H) 101
Table 55 — MR8 Definition 101
Table 56 — MR9 Register Information (MA[7:0] = 09_H) 101
Table 57 — MR9 Definition 101
Table 58 — MR10 Register Information (MA [7:0] = $0A_H$) 102
Table 59 — MR10 Definition 102
Table 60 — MR11 Register Information (MA[7:0] = $0B_H$) 103
Table 61 — MR11 Definition 103
Table 62 — MR12 Register Information (MA[5:0] = $0C_H$) 104
Table 63 — MR12 Definition 104
Table 64 — MR12 V_{REF}(CA) Settings 105
Table 65 — MR13 Register Information (MA[5:0] = $0D_H$) 106
Table 66 — MR13 Definition 106
Table 67 — MR14 Register Information (MA[7:0] = $0E_H$) 107
Table 68 — MR14 definition 107
Table 69 — MR14 V_{REF}(DQ[7:0]) Settings 108
Table 70 — MR15 Register Information (MA[7:0] = $0F_H$) 109
Table 71 — MR15 definition 109
Table 72 — MR15 VREF(DQ[15:8]) Settings 110
Table 73 — MR16 Register Information (MA[5:0] = 10_H) 111
Table 74 — MR16 definition 111
Table 75 — MR17 Register Information (MA[5:0] = 11_H) 112
Table 76 — MR17 definition 112
Table 77 — MR18 Register Information (MA[7:0] = 12_H) 113
Table 78 — MR18 Definition 113
Table 79 — MR19 Register Information (MA[7:0] = 13_H) 114
Table 80 — MR19 Definition 114
Table 81 — MR20 Register Information (MA[7:0] = 14_H) 115
Table 82 — MR20 definition 115
Table 83 — MR21 Register Information (MA[7:0] = 15_H) 116
Table 84 — MR21 Definition 116
Table 85 — MR22 Register Information (MA[7:0] = 16_H) 117
Table 86 — MR22 Definition 117
Table 87 — MR23 Register Information (MA[5:0] = 17H) 117
Table 88 — MR23 Definition 117
Table 89 — Row Address of Masked Segment for x16 Mode 117
Table 90 — Row Address of Masked Segment for x8 Mode 117
Table 91 — MR24 Register Information (MA[5:0] = 18H) 118
Table 92 — MR24 Definition 118
Table 93 — MR25 Register Information (MA[7:0] = 19_H) 119
Table 94 — MR25 Definition 119
Table 95 — MR26 Register Information (MA[7:0] = $1A_H$) 119

Contents (cont'd)

Table 96 — MR26 definition........119
Table 97 — MR27 Register Information (MA[7:0] = $1B_H$)........120
Table 98 — MR27 Definition........120
Table 99 — MR28 Register Information (MA[7:0] = $1C_H$)........121
Table 100 — MR28 Definition........121
Table 101 — MR29 Register Information (MA[7:0] = 1DH)........122
Table 102 — MR29 Definition........122
Table 103 — MR30 Register Information (MA[5:0] = $1E_H$)........123
Table 104 — MR30 Definition........123
Table 105 — MR31 Register Information (MA[7:0] = $1F_H$)........124
Table 106 — MR31 Definition........124
Table 107 — MR31 Invert Register Pin Mapping........124
Table 108 — MR32 Register Information (MA[7:0] = 20_H)........125
Table 109 — MR32 definition........125
Table 110 — MR32 Invert Register Pin Mapping........125
Table 111 — MR33 Register Information (MA[7:0] = 21_H)........126
Table 112 — MR33 Definition........126
Table 113 — MR34 Register Information (MA[7:0] = 22_H)........126
Table 114 — MR34 Definition........126
Table 115 — MR35 Register Information (MA[7:0] = 23_H)........127
Table 116 — MR35 Definition........127
Table 117 — MR36 Register Information (MA[7:0] = 24_H)........127
Table 118 — MR36 Definition........127
Table 119 — MR37 Register Information (MA[7:0] = 25_H)........128
Table 120 — MR37 Definition........128
Table 121 — MR38 Register Information (MA[7:0] = 26_H)........129
Table 122 — MR38 Definition........129
Table 123 — MR39 Register Information (MA[7:0] = 27_H)........129
Table 124 — MR39 Definition........129
Table 125 — MR40 Register Information (MA[7:0] = 28_H)........130
Table 126 — MR40 Definition........130
Table 127 — MR41 Register Information (MA[7:0] = 29_H)........131
Table 128 — MR42 Register Information (MA[7:0] = $2A_H$)........131
Table 129 — MR42 definition........131
Table 130 — MR43 Register Information (MA[7:0] = $2B_H$)........132
Table 131 — MR43 definition........132
Table 132 — MR44 Register Information (MA[7:0] = $2C_H$)........133
Table 133 — MR44 definition........133
Table 134 — MR45 Register Information (MA[7:0] = $2D_H$)........134
Table 135 — MR45 definition........134
Table 136 — MR46 Register Information (MA[5:0] = $2E_H$)........134
Table 137 — MR46 definition........134
Table 138 — MR47 Register Information (MA[7:0] = $2F_H$)........135
Table 139 — MR47 Definition........135
Table 140 — MR48 Register Information (MA[7:0] = 30_H)........135
Table 141 — MR48 Definition........135
Table 142 — MR49 Register Information (MA[7:0] = 31_H)........135
Table 143 — MR49 Definition........135
Table 144 — MR50 Register Information (MA[7:0] = 32_H)........135
Table 145 — MR50 Definition........135
Table 146 — MR51 Register Information (MA[7:0] = 33_H)........135
Table 147 — MR51 Definition........135
Table 148 — MR52 Register Information (MA[7:0] = 34_H)........136
Table 149 — MR52 Definition........136

Contents (cont'd)

Table 150 — MR53 Register Information (MA[7:0] = 35_H)........136
Table 151 — MR53 Definition........136
Table 152 — MR54 Register Information (MA[7:0] = 36H)........136
Table 153 — MR54 Definition........136
Table 154 — Command Truth Table........137
Table 155 — Allowable CAS command operand(s) combination........139
Table 156 — CAS command with WCK2CK Synchronization bits........140
Table 157 — WCK2CK Sync AC Parameters for WRITE operation........142
Table 158 — WCK2CK Sync AC Parameters for Read operation........144
Table 159 — WCK2CK Sync AC Parameters for Read operation........145
Table 160 — WCK2CK Sync AC Parameters for Read operation........145
Table 161 — WCK2CK Sync AC Parameters for CAS(WS_FAST)........147
Table 162 — WCK2CK SYNC Off Timing Definition (16B Mode) for WR16/32, RD16/32 and MWR........149
Table 163 — WCK2CK SYNC Off Timing Definition (BG Mode) for WR16/32, RD16/32 and MWR........150
Table 164 — WCK2CK SYNC Off Timing Definition (8B Mode) for WR16/32, RD16/32 and MWR........151
Table 165 — WCK2CK SYNC Off Timing Definition for MRR........152
Table 166 — WCK2CK SYNC Off Timing Definition for Training Commands........153
Table 167 — WCK buffer off CAS command (Allowed only when MR18 OP[4]=1)........161
Table 168 — Precharge Bank Selection 8 Bank mode........165
Table 169 — Precharge Bank Selection 4 Bank / 4 Bank Group mode........166
Table 170 — Precharge Bank Selection 16 Banks mode........166
Table 171 — Timing Between Commands (PRECHARGE and Auto-PRECHARGE) : DQ ODT is Disable........173
Table 172 — Core Timing (tRBTP)........178
Table 173 — RDQS Timing Parameters........182
Table 174 — RDQS Pattern Definition in case READ to READ command timing is BL/n + k*nCK (k=1, 2)........183
Table 175 — RDQS Pattern Definition in case READ to READ command timing delay is BL/n + k*nCK (k=1, 2, 3)........184
Table 176 — Read Latencies for Link ECC off case (DVFSC disabled)........189
Table 177 — Read Latencies for Link ECC off case (DVFSC enabled)........190
Table 178 — Write Latency: DVFSC Disabled........191
Table 179 — Write Latency: DVFSC Enabled........191
Table 180 — nWR Latency........193
Table 181 — tCCDMW........195
Table 182 — DMI pin behavior by command and support function setting........201
Table 183 — DMI pin behavior by command and support function setting........203
Table 184 — Bank and Refresh counter increment behavior on the 4Bank/4BG mode or 16Bank mode........205
Table 185 — Bank and Refresh counter increment behavior on the 8bank mode........206
Table 186 — REFRESH Command Scheduling Separation requirements for 4Bank /4BG mode or 16Bank mode........207
Table 187 — REFRESH Command Scheduling Separation requirements for 8Bank mode........208
Table 188 — REFRESH Command Timing Constraints........210
Table 189 — Refresh Requirement Parameters for BG mode or 16Bank mode........211
Table 190 — Refresh Requirement Parameters for 8Bank mode........212
Table 191 — Self Refresh AC Timing........217
Table 192 — Self Refresh Exit (SRX) Command Timing Constraints........218
Table 193 — Example of Segment Masking use in LPDDR5 SDRAM........219
Table 194 — Mode Register Read/Write AC Timing........225
Table 195 — Deep Sleep Mode AC Timing Table........227

Contents (cont'd)

Table 196 — DQ Output Mapping for lower byte 228
Table 197 — DQ Output Mapping for upper byte 229
Table 198 — Mode Register Read/Write AC Timing 232
Table 199 — Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW) 233
Table 200 — Mode Register Function with three physical registers 234
Table 201 — Relation between MR Setting and DRAM Operation 235
Table 202 — Frequency Set Point AC Timing Table 236
Table 203 — tFC value mapping 236
Table 204 — tFC value mapping example 236
Table 205 — Command/Address Bus ODT State 240
Table 206 — ODT DC Electrical Characteristics, assuming RZQ = 240Ω±1% over the entire operating temperature range after a proper ZQ calibration 241
Table 207 — ODT Command/Address bus AC timing parameter 242
Table 208 — ODTLon and ODTLoff Latency Values 244
Table 209 — Asynchronous ODT Turn On and Turn Off Timing 245
Table 210 — ODT DC Electrical Characteristics, assuming RZQ = 240Ω±1% over the entire operating temperature range after a proper ZQ calibration 246
Table 211 — Non-target and Target ODT status depending on DRAM state 248
Table 212 — Normal Mode vs. NT-ODT Mode for Write Operation 249
Table 213 — Normal Mode vs. NT-ODT Mode for Read Operation 249
Table 214 — Combination of Target ODT, Non-target ODT and SoC ODT 250
Table 215 — DQ ODT setting example for Write Operation in NT-ODT Mode 251
Table 216 — ODTLon and ODTLoff Latency Values for Write 253
Table 217 — Asynchronous NT-ODT Turn On and Turn off Timing for Write 253
Table 218 — ODTLon_RD and ODTLoff_RD Latency Values for Read with RDQS disabled 254
Table 219 — ODTLon_RD and ODTLoff_RD Latency Values for Read with RDQS enabled & MR10 OP[5:4]=00_B, 01_B, 10_B 255
Table 220 — ODTLon_RD and ODTLoff_RD Latency Values for Read with RDQS enabled & MR10 OP[5:4]=11_B 256
Table 221 — Asynchronous NT-ODT Turn On and Turn Off Timing 256
Table 222 — VRCG Enable / Disable Timing 258
Table 223 — Temperature Sensor 260
Table 224 — MPC Command Definition 261
Table 225 — MPC Command Definition for OP[7:0] 261
Table 226 — WCK Oscillator Matching Error Specification 264
Table 227 — VDDQ Ramp Rates 271
Table 228 — Reference data S[7:0] bit mapping 272
Table 229 — Write data copy hit or miss operands (DC0 – DC3) of CAS command 272
Table 230 — Read data copy function 273
Table 231 — CAS command with write X (zero) enable bits. 275
Table 232 — AC Timing 278
Table 233 — MR29 OP[7:0] Register Information 278
Table 234 — Combination of PPR Resource for CA Input 278
Table 235 — Guard Key Encoding for MR42 279
Table 236 — PPR Timing Parameters 281
Table 237 — ECC Check Matrix for Data 286
Table 238 — ECC Check Matrix for DMI 287
Table 239 — Allowable combination among CK_t/c, WCK_t/c and RDQS_t/c 291
Table 240 — Restriction of Single-ended mode for MR1 and MR20 292
Table 241 — SE from/to Differential FSP and additional period for MRW AC timing 295
Table 242 — Delta CK and DQS Specification 295
Table 243 — Effective Burst Length (BL/n) Definition 296
Table 244 — Command Timing Constraints for Same Banks in Same Bank Group (DQ ODT is disabled) 297

Contents (cont'd)

Table 245 — Command Timing Constraints for Different Banks in Same Bank Group DQ ODT is disabled) ... 298
Table 246 — Command Timing Constraints for Different Banks in Different Bank Group (DQ ODT is disabled) ... 298
Table 247 — Command Timing Constraints for Same Banks in 8B Mode (DQ ODT is disabled) ... 299
Table 248 — Command Timing Constraints for Different Banks in 8B Mode (DQ ODT is disabled) ... 299
Table 249 — Command Timing Constraints for Same Banks in 16B Mode (DQ ODT is disabled) ... 300
Table 250 — Command Timing Constraints for Different Banks in 16B Mode (DQ ODT is disabled) ... 300
Table 251 — Command Timing Constraints for Same Banks in Same Bank Group (DQ ODT is enabled) ... 301
Table 252 — Command Timing Constraints for Different Banks in Same Bank Group (DQ ODT is enabled) ... 301
Table 253 — Command Timing Constraints for Different Banks in Different Bank Group (DQ ODT is enabled) ... 301
Table 254 — Command Timing Constraints for Same Banks in 8B Mode (DQ ODT is enabled) ... 302
Table 255 — Command Timing Constraints for Different Banks in 8B Mode (DQ ODT is enabled) ... 302
Table 256 — Command Timing Constraints for Same Banks in 16B Mode (DQ ODT is enabled) ... 303
Table 257 — Command Timing Constraints for Different Banks in 16B Mode (DQ ODT is enabled) ... 303
Table 258 — Auto Precharge Command Timing Constraints for Same Banks in Same Bank Group ... 304
Table 259 — Command Timing Constraints for Different Banks in Same Bank Group (DQ ODT Disabled) ... 304
Table 260 — Command Timing Constraints for Different Banks in Different Bank Group (DQ ODT Disabled) ... 304
Table 261 — Command Timing Constraints for Same Banks in 8B Mode ... 305
Table 262 — Command Timing Constraints for Different Banks in 8B Mode (DQ ODT Disabled) ... 305
Table 263 — Command Timing Constraints for Same Banks in 16B Mode ... 305
Table 264 – Command Timing Constraints for Different Banks in 16B Mode (DQ ODT Disabled) ... 306
Table 265 — Command Timing Constraints for Different Banks in Same Bank Group (DQ ODT Enabled) ... 306
Table 266 — Command Timing Constraints for Different Banks in Different Bank Group (DQ ODT Enabled) ... 306
Table 267 — Command Timing Constraints for Different Banks in 8B Mode (DQ ODT Enabled) ... 307
Table 268 — Command Timing Constraints for Different Banks in 16B Mode (DQ ODT Enabled) ... 307
Table 269 — CAS (WS_FS) Command Timing Constraints ... 308
Table 270 — CAS (WS_WR) Command Timing Constraints ... 309
Table 271 — CAS (WS_RD) Command Timing Constraints ... 310
Table 272 — CAS (WS_OFF) Command Timing Constraints ... 311
Table 273 — CAS (DC0-3), CAS (WRX) Command Timing Constraints ... 312
Table 274 — CAS (B3) Command Timing Constraints ... 313
Table 275 — CAS(WS_FS), CAS(WS_WR), CAS(WS_RD), CAS(WS_OFF) Command Timing Constraints ... 314

Contents (cont'd)

Table 276 — CAS(DC0-3), CAS(WRX) Command Timing Constraints 315
Table 277 — CAS (B3) Command Timing Constraints 316
Table 278 —Training-Related Timing Constraints 317
Table 279 — MRR/MRW Timing Constraints: DQ ODT is Disable 318
Table 280 — MRR/MRW Timing Constraints: DQ ODT is Enable 319
Table 281 — Command Timing Constraints in case of Different Ranks, ODT ON, CAS-WS_FS Broadcast ON 320
Table 282 — Command Timing Constraints in case of Different Ranks, ODT OFF, CAS-WS_FS Broadcast ON 321
Table 283 — Command Timing Constraints in case of Different Ranks, ODT ON, CAS-WS_FS Broadcast OFF 322
Table 284 — Command Timing Constraints in case of Different Ranks, ODT OFF, CAS-WS_FS Broadcast OFF 322
Table 285 — x16 Core Timing for BG mode: DVFSC Disabled & Link ECC Disabled 323
Table 286 — x16 Core Timing for 16B mode: DVFSC Disabled & Link ECC Disabled 323
Table 287 — x16 Core Timing for 8B mode: DVFSC Disabled & Link ECC Disabled 323
Table 288 — Byte Mode Core Timing for BG mode: DVFSC Disabled & Link ECC Disabled 324
Table 289 — Byte Mode Core Timing for 16B mode: DVFSC Disabled & Link ECC Disabled 324
Table 290 — Byte Mode Core Timing for 8B mode: DVFSC Disabled & Link ECC Disabled 324
Table 291 — x16 Core Timing for BG mode: DVFSC Disabled & Link ECC Enabled 325
Table 292 — x16 Core Timing for 16B mode: DVFSC Disabled & Link ECC Enabled 325
Table 293 — x16 Core Timing for 8B mode: DVFSC Disabled & Link ECC Enabled 325
Table 294 — Byte Mode Core Timing for BG mode: DVFSC Disabled & Link ECC Enabled 326
Table 295 — Byte Mode Core Timing for 16B mode: DVFSC Disabled & Link ECC Enabled 326
Table 296 — Byte Mode Core Timing for 8B mode: DVFSC Disabled & Link ECC Enabled 326
Table 297 — x16 Core Timing for 16B mode: DVFSC Enabled & Link ECC Disabled 327
Table 298 — x16 Core Timing for 8B mode: DVFSC Enabled & Link ECC Disabled 327
Table 299 — Byte Mode Core Timing for 16B mode: DVFSC Enabled & Link ECC Disabled 327
Table 300 — Byte Mode Core Timing for 8B mode: DVFSC Enabled & Link ECC Disabled 327
Table 301 — Temperature Derating AC Timing 328
Table 302 — Absolute Maximum DC Ratings 329
Table 303 — Recommended DC Operating Conditions 330
Table 304 — Input Leakage Current 332
Table 305 — Input/Output Leakage Current 332
Table 306 — Operating Temperature Range 332
Table 307 — Operating Temperature Range 333
Table 308 — Electrostatic Discharge Sensitivity Characteristics 333
Table 309 — Reset input level specification 334
Table 310 — LPDDR5 Input Level for CS 334
Table 311 — AC Overshoot / Undershoot 334
Table 312 — LPDDR5 AC Overshoot / Undershoot for LVSTL 334
Table 313 — CK Differential Input Voltage 336
Table 314 — Clock Single-Ended Input Voltage 337
Table 315 — Differential Input Slew Rate Definition for CK_t, CK_c 338
Table 316 — Differential Input Level for CK_t, CK_c 338
Table 317 — Differential Input Slew Rate for CK_t, CK_c 338
Table 318 — Cross point voltage for differential input signals (Clock) 339
Table 319 — WCK differential input voltage 340
Table 320 — WCK Single-Ended Input Voltage 342
Table 321 — Differential Input Slew Rate Definition for WCK_t, WCK_c 343
Table 322 — Differential Input Level for WCK_t, WCK_c 343
Table 323 — Differential Input Slew Rate for WCK_t, WCK_c 343
Table 324 — Cross point voltage for differential input signals (WCK) 344
Table 325 — Output Slew Rate (single-ended) 345

Contents (cont'd)

Table 326 — Differential Output Slew Rate 346
Table 327 — Single Ended WCK parameters 348
Table 328 — Single Ended CK parameters 349
Table 329 — Reference Voltage for tLZ(RDQS), tHZ(RDQS) Timing Measurements 351
Table 330 — Reference Voltage for tLZ(DQ), tHZ(DQ) Timing Measurements 353
Table 331 — Read AC Timing 354
Table 332 — Input / Output Capacitance 355
Table 333 — Definition of Switching for CA Input Signals 356
Table 334 — CA Pattern for IDD4R @ BG mode 356
Table 335 — CA Pattern for IDD4R @ 16B mode 357
Table 336 — CA Pattern for IDD4R @ 8B mode 357
Table 337 — CA Pattern for IDD4W@ BG mode 358
Table 338 — CA Pattern for IDD4W @ 16B mode 358
Table 339 — CA Pattern for IDD4W@ 8B mode 359
Table 340 — Data Pattern for IDD4R @ DBI Off 360
Table 341 — Data Pattern for IDD4W @ DBI Off 362
Table 342 — Data Pattern for IDD4R @ DBI On 363
Table 343 — Data Pattern for IDD4W @ DBI On 365
Table 344 — LPDDR5 IDD Specification Parameters and Operating Conditions 366
Table 345 — Clock AC Timings for 5/10/67/133MHz 371
Table 346 — Clock AC Timings for 200/267/344/400MHz 372
Table 347 — Clock AC Timings for 467/533/600/688 372
Table 348 — Clock AC Timings for 750/800MHz 372
Table 349 — Write Clock AC Timings for 266/533/800/1067MHz 375
Table 350 — Write Clock AC Timings for 1375/1600/1867/2134MHz 376
Table 351 — Write Clock AC Timings for 2400/2750/3000/3200MHz 376
Table 352 — DRAM DQ output timing 379
Table 353 — CS Rx Specification 382
Table 354 — CA Rx Specification 385
Table 355 — DQ, DMI, Parity and DBI Rx Specification 389
Table 356 — Pull-down Driver Characteristics, with ZQ Calibration 390

Tables

Table 357 — Pull-Up Characteristics, with ZQ Calibration 390
Table 358 — Valid Calibration Points 390
Table 359 — Un-terminated Pull Up Characteristics 390
Table 360 — Worst Case Output Driver and Termination Resistance 391
Table 361 — Worst Case Output high voltage 391
Table 362 — Output Driver and Termination Resistance Temperature and Voltage Sensitivity 392
Table 363 — LPDDR5 Pad order 394
Table 364 — Package configuration example 395

LOW POWER DOUBLE DATA RATE (LPDDR) 5

(From JEDEC Board Ballet JCB-18-50, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memories.)

1 Scope

This document defines the LPDDR5 standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a JEDEC compliant x16 one channel SDRAM device and x8 one channel SDRAM device. LPDDR5 device density ranges from 2 Gb through 32 Gb. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), DDR4 (JESD79-4), LPDDR (JESD209), LPDDR2 (JESD209-2), LPDDR3 (JESD209-3) and LPDDR4 (JESD209-4).

Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the LPDDR5 standard.