

JEDEC STANDARD

THERMAL TEST CHIP GUIDELINE (WIRE BOND AND FLIP CHIP)

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Introduction

Thermal Test Chips have three primary purposes in the area of semiconductor device packaging:

- 1) To provide a well-defined structure for the generation of heat flux with built-in temperature sensor(s) that can be used to compare the thermal performance of semiconductor packages,
- 2) To use the well-defined structure in a specific package for validating or calibrating thermal model simulations, and
- 3) To provide a vehicle for thermal investigation of power topology mapping, power transient response, and complex packaging assemblies that would be difficult to accomplish using an application semiconductor device.

THERMAL TEST CHIP GUIDELINE (WIRE BOND AND FLIP CHIP)

(From JEDEC Board Ballot JCB-19-11, formulated under the cognizance of the JC-15 Committee on Thermal Characterization Techniques for Semiconductor Packages.)

1 Scope

The purpose of this document is to provide a design guideline for thermal test chips used for integrated circuit (IC) and transistor package thermal characterization and investigations. The intent of this guideline is to minimize the differences in data gathered due to nonstandard test chips and to provide a well-defined reference for thermal investigations.

The thermal test chips described in this document will apply to single and multiple chip devices. These are designed using standard semiconductor wafer fabrication processes and can be used with a wide variety of industry standard packages. These test chips can operate in a static mode in which constant power is continuously supplied to the device while monitoring the temperature through the measurement of a Temperature Sensitive Parameter (TSP). They can also operate in a transient mode in which the power supply and the TSP are monitored as a function of time (t). This guideline covers test chips meant to be both wire bonded or flip chip bumped to the package external contacts.

1.1 Rationale

The thermal resistance for a specific device varies with many factors. The chip size, location and size of the power dissipation element(s), and location of the temperature sensor(s) will directly affect the thermal test results. It is essential to standardize thermal test chip design guideline in order to provide meaningful measurement results. This allows semiconductor suppliers to compare different packages over a wide variety of conditions, such as power levels and air flows. It will also help the users to estimate their active device junction temperature under actual operating conditions by allowing them to extrapolate the results of a defined standard condition.