JEDEC STANDARD

Byte Addressable Energy Backed Interface

JESD245C

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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BYTE ADDRESSABLE ENERGY BACKED INTERFACE

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Foreword

This standard has been prepared by JEDEC. The purpose of this standard is definition of a byte addressable energy backed function on a non-volatile dual in-line memory module (NVDIMM). This standard defines the feature set and commands implemented by the byte addressable energy backed function on an NVDIMM-N.

Introduction

An NVDIMM-N is a memory module that can be integrated into a standard platform. A Byte Addressable Energy Backed Function on a NVDIMM is designed to preserve data in the event of the power failure. A Byte Address Energy Backed Function is backed by a combination of SDRAM and non-volatile memory (e.g., NAND flash) on the NVDIMM-N. It operates at SDRAM speeds and provides persistent storage by backing up the SDRAM contents into the non-volatile memory in the event of a power failure or other triggers. This is made possible by an Energy Source (e.g., supercapacitor) which maintains charge on the module enabling back-up of data from SDRAM to the non-volatile memory (NVM), providing a storage-class memory solution. The module may also support the ability to encrypt the SDRAM contents before backing up to the NVM.

To be able to provide interoperability and the ability for platform and platform software (e.g., BIOS) to support NVDIMM-Ns from various manufacturers, standardization of the host to module interface, discovery mechanism, the feature set and command operations are required, as described in this standard.

BYTE ADDRESSABLE ENERGY BACKED INTERFACE

(From JEDEC Board Ballot JCB-19-18, formulated under the cognizance of the JC-45.6 Subcommittee on Hybrid Modules)

1 Scope

This standard specifies the host and device interface for a DDR4 NVDIMM-N, which is a DIMM that achieves non-volatility by copying SDRAM contents into non-volatile memory (NVM) when host power is lost using an Energy Source managed by either the module or the host.

Although this standard is targeted towards DDR4 NVDIMM only, it does not preclude adoption of this standard by other implementations (e.g., DDR3 NVDIMM).

2 Normative references

2.1 Overview

The normative documents listed in this clause contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated. For undated references, the latest edition of the normative document referred to applies.

2.2 JEDEC standards

JESD21C, 4.20.28, *DDR4 SDRAM Registered DIMM Design Specification*, Revision 1.00 (August 2015)

JESD21C, 4.1.2.L-4, *Annex L: Serial Presence Detect (SPD) for DDR4 SDRAM Modules* (DDR4 SPD Document Release 4)

JESD21C, 4.1.6, *Definitions of the EE1004-v 4 Kbit Serial Presence Detect (SPD) EEPROM and TSE2004av 4 Kbit SPD EEPROM with Temperature Sensor (TS) for Memory Module Applications*

JESD79-4B, *DDR4 SDRAM* (June 2017)

JESD82-31, *DDR4 Registering Clock Driver – DDR4RCD01* (August 2016)

JESD82-31A, *DDR4 Registering Clock Driver – DDR4RCD02* (forthcoming)

JESD82-32, *DDR4 Data Buffer – DDR4DB01* (August 2016)

JESD82-32A, *DDR4 Data Buffer – DDR4DB02* (forthcoming)

JESD245, *Byte Addressable Energy Backed Interface* (December 2015)

JESD245A, *Byte Addressable Energy Backed Interface* (September 2016)

JESD245B.01, *Byte Addressable Energy Backed Interface* (September 2017)

JESD248A, *DDR4 NVDIMM-N Design Specification* (March 2018)

2.3 Management interface standards

I^2C Bus Specification Revision 6 (4 April 2014)

System Management Bus (SMBus) Specification Version 3.0 (20 December 2014)