

The documentation and process conversion measures necessary to comply with this revision shall be completed by 23 August 2019.

## PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, NPN, SILICON, POWER,  
TYPE 2N3879, QUALITY LEVELS JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

## 1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN, silicon, power transistors. Three levels of product assurance (JAN, JANTX, and JANTXV) are provided for each device type as specified in [MIL-PRF-19500](#).

1.2 Package outline. The device package outline is a modified TO-213AA (similar to a TO-66) in accordance with [figure 1](#).

1.3 Maximum ratings. Unless otherwise specified,  $T_A = +25^\circ\text{C}$ .

$P_T$ (1) $T_C = +25^\circ\text{C}$	$R_{\theta\text{JC}}$	$V_{\text{CBO}}$	$V_{\text{CEO}}$	$V_{\text{EBO}}$	$I_B$	$I_C$	$T_J$ and $T_{\text{STG}}$
<u>W</u>	<u><math>^\circ\text{C/W}</math></u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u><math>^\circ\text{C}</math></u>
35	5	120	75	7	5	7	-65 to +200

(1) Derate linearly 200 mW/ $^\circ\text{C}$  for  $T_C > +25^\circ\text{C}$ .

## 1.4 Primary electrical characteristics.

	$h_{\text{FE1}}$ (1) $V_{\text{CE}} = 5.0 \text{ V dc}$ $I_C = 0.5 \text{ A dc}$	$h_{\text{FE2}}$ (1) $V_{\text{CE}} = 5.0 \text{ V dc}$ $I_C = 4.0 \text{ A dc}$	$V_{\text{BE(SAT)1}}$ $I_C = 4.0 \text{ A dc}$ $I_B = 0.4 \text{ A dc}$	$V_{\text{CE(SAT)1}}$ $I_C = 4.0 \text{ A dc}$ $I_B = 0.4 \text{ A dc}$	$C_{\text{obo}}$ $V_{\text{CB}} = 10 \text{ V dc}$ $I_E = 0$ $0.1 \text{ MHz} \leq f \leq 1 \text{ MHz}$	$ h_{\text{re}} $ $V_{\text{CE}} = 10 \text{ V dc}$ $I_C = 500 \text{ mA dc}$ $f = 10 \text{ MHz}$	Switching (see <a href="#">table 1</a> and <a href="#">figure 2</a> herein)	
							$t_{\text{on}}$	$t_{\text{off}}$
Min	40	20	<u>V dc</u>	<u>V dc</u>	<u>pF</u>	4	<u><math>\mu\text{s}</math></u>	<u><math>\mu\text{s}</math></u>
Max		80	2.0	1.2	175	20	0.44	1.2

(1) Pulsed (see [4.5.1](#)).

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.

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