JEDEC STANDARD

Low Power Double Data Rate 5 (LPDDR5)

JESD209-5A

(Revision of JESD209-5, December 2018)

January 2020

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2020
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

PRICE: Contact JEDEC

Printed in the U.S.A.

Contents

Figures

Tables

LOW POWER DOUBLE DATA RATE 5 (LPDDR5)

(From JEDEC Board Ballot JCB-19-32, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memories (Item 1854.99A).)

1 Scope

This document defines the LPDDR5 standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a JEDEC compliant x16 one channel SDRAM device and x8 one channel SDRAM device. LPDDR5 device density ranges from 2 Gb through 32 Gb. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), DDR4 (JESD79-4), LPDDR (JESD209), LPDDR2 (JESD209-2), LPDDR3 (JESD209-3) and LPDDR4 (JESD209-4).

Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the LPDDR5 standard.

2 Overview

2.1 Features

TBD

2.2 Functional Description

LPDDR5 SDRAM is a high-speed synchronous SDRAM device internally configured with 1 channel containing either 16 or 8 DQ signals. The bank architecture is user-selectable, and can be either eight banks (8B Mode), four banks with four bank groups (BG Mode), or sixteen banks (16B Mode). See 2.2.3 for more information.

Density can range from 2Gb to 32Gb. These LPDDR5 SDRAM devices contain the following number of bits:

- 2Gb has 2,147,483,648 bits
- 3Gb has 3,221,225,472 bits
- 4Gb has 4,294,967,296 bits
- 6Gb has 6,442,450,944 bits
- 8Gb has 8,589,934,592 bits
- 12Gb has 12,884,901,888 bits
- 16Gb has 17,179,869,184 bits
- 24Gb has 25,769,803,776 bits
- 32Gb has 34,359,738,368 bits

LPDDR5 SDRAM devices use a command clock (CK) that operates at a reduced rate from per-byte data clock (WCK). There are seven (DDR) command/address (CA) pins that the memory controller uses to transmit command, address, bank, configuration, and training information to the SDRAM. CA signals are latched on both the rising and falling CK edges when indicated by a high signal on the single (SDR) CS pin. Most commands are 1 nCK in duration. See Table 179 for details.

The WCK:CK ratio is user-selectable as either 2:1 or 4:1. For low-power operation the WCK is generally designed to operate only when read or write data needs to be transmitted on the bus. Due to the high speeds required for WCK, the LPDDR5 SDRAM generally implements circuitry to divide the WCK frequency immediately after the WCK receiver. This leads to a requirement to synchronize WCK to CK when the WCK needs to be re-started from an idle time. See 7.2.1 for details.