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UNIVERSAL FLASH STORAGE (UFS), VERSION 3.1

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Foreword

This standard has been prepared by JEDEC. The purpose of this standard is definition of a UFS Universal Flash Storage electrical interface and a UFS memory device. This standard defines a unique UFS feature set and includes the feature set of eMMC standard as a subset. This standard references several other standard specifications by MIPI (M-PHY and UniPro specifications) and INCITS T10 (SBC, SPC and SAM draft standards) organizations.

Introduction

The UFS electrical interface is a universal serial communication bus which can be utilized for different types of applications. It's based on MIPI M-PHY specification as physical layer for optimized performance and power. The UFS architectural model references the INCITS T10 SAM model for ease of adoption.

The UFS device is a universal data storage and communication media. It is designed to cover a wide area of applications as smart phones, cameras, organizers, PDAs, digital recorders, MP3 players, internet tablets, electronic toys, etc.

UNIVERSAL FLASH STORAGE (UFS), VERSION 3.1

(From JEDEC Board Ballot JCB-19-31, formulated under the cognizance of the JC-64.1 Subcommittee on Electrical Specifications and Command Protocols, Item 135.99)

1 Scope

This standard specifies the characteristics of the UFS electrical interface and the memory device. Such characteristics include (among others) low power consumption, high data throughput, low electromagnetic interference and optimization for mass memory subsystem efficiency. The UFS electrical interface is based on an advanced differential interface by MIPI M-PHY specification which together with the MIPI UniPro specification forms the interconnect of the UFS interface. The architectural model is referencing the INCITS T10 (SCSI) SAM standard and the command protocol is based on INCITS T10 (SCSI) SPC and SBC standards.

2 Normative Reference

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated. For undated references, the latest edition of the normative document referred to applies.

[MIPI-M-PHY], *MIPI Alliance Specification for M-PHY[®], Version 4.1, 28 March 2017*

[MIPI-UniPro], *MIPI Alliance Specification for Unified Protocol (UniPro[®]), Version 1.8, 11 January 2018*

[MIPI-DDB], *MIPI Alliance Specification for Device Descriptor Block (DDB), Version 1.0*

[MIPI-AP], *Application Note for UniPro[®] v1.8*

[SAM], *INCITS T10 draft standard: SCSI Architecture Model – 5 (SAM–5), Revision 05, 19 May 2010*

[SPC], *INCITS T10 draft standard: SCSI Primary Commands – 4 (SPC-4), Revision 27, 11 October 2010*

[SBC], *INCITS T10 draft standard: SCSI Block Commands – 3 (SBC–3), Revision 24, 05 August 2010*

[JESD8-12A], *1.2 V +/- 0.1V (Normal Range) and 0.8 - 1.3 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits*

[HBM-MM], *JEDEC Recommended ESD Target Levels for HBM/MM Qualification, JEP155A.01, March 2012*

[CDM], *JEDEC Recommended ESD-CDM Target Levels, JEP157, October 2009*

[HMAC-SHA], *Eastlake, D. and T. Hansen, US Secure Hash Algorithms (SHA and HMAC-SHA), RFC 4634, July 2006.*

[JEP106], *Standard Manufacturer's identification code, JEP106*

[JESD21C], *Multichip Packages (MCP) and Discrete eMMC, e2MMC, and UFS*

[JESD220-3], *UFS Host Performance Booster (HPB) Extension Specification*