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GUIDELINE FOR SWITCHING RELIABILITY EVALUATION PROCEDURES FOR GALLIUM NITRIDE POWER CONVERSION DEVICES

Contents

Foreword

This document was drafted by the JEDEC JC-70.1 GaN Power Electronics Conversion Semiconductor Standards subcommittee consisting of worldwide industry experts from various power semiconductor, power supply and test equipment manufacturing companies.

The early efforts for this document development were started in 2016 in the GaN Standards for Power Electronic Conversion Devices Working Group (GaNSPEC DWG). GaNSPEC DWG was an independent working body that later transitioned into JC-70.1 in 2017 and consisted of industry experts along with academics located around the globe.

This document is intended for use by GaN product suppliers and related power electronic industries. It provides guidelines for evaluating the switching reliability of GaN power switches and assuring their reliable use in power conversion applications. It is applicable to planar enhancement-mode, depletion-mode, GaN integrated power solutions and cascode GaN power switches.

Introduction

Gallium Nitride (GaN) power switches are important devices for high-efficiency, small form-factor power conversion applications. Current GaN power switches are based upon the planar High Electron Mobility Transistor (HEMT), which is a Field-Effect Transistor (FET). The switch may be a discrete enhancement or depletion-mode GaN FET, a GaN FET in combination with a silicon transistor forming a cascode and/or co-packaged with silicon control electronics. It may also be a GaN power FET with integrated GaN electronics. During operation, all power devices experience switching stress for which the reliability needs to be evaluated and lifetimes assured.

For many silicon power conversion products, operational robustness is often validated by a combination of technology and product-level tests, e.g., Hot Carrier Injection (HCI) [1], Unclamped Inductive Switching (UIS) [2], high-temperature operating life (HTOL) [3]. Individual silicon tests do not necessarily validate operation under actual-use conditions of power conversion products, which simultaneously involve high power transfer through the device, high slew rates, and hot-carrier effects. Each addresses different aspects, and over the years they have been developed to work well together. These tests are either not applicable or have not been comprehensively specified for GaN switches. For example, the HCI test relies on a body contact that is not available in GaN FETs and the UIS test takes the device into avalanche, which is not recommended for GaN FETs. The GaN industry has therefore been conducting switching reliability testing to assure the reliability and robustness of GaN switches [4]-[8], both at the technology level and in application.

Introduction (cont'd)

The industry and research community now need to work towards standardizing the methodology for assuring both the switching reliability of the technology platform and the robustness of GaN switches for use in a broad class of power management applications. Typically, standards lag technology introduction because there needs to be substantial public knowledge of failure modes and mechanisms before a standards document can be published. This takes time because confidential information needs to be de-classified and new knowledge discovered. It is, however, desirable for the industry to develop common approaches sooner, so that customers can readily evaluate the technology options available. The goal of this document is to present guidelines for a common approach, and to accelerate progress towards the future standard.

A common approach for power management needs to consider many aspects. Power conversion involves different modes of operation, e.g., hard and soft-switching, the usage of the power switch in many different topologies, and the interaction of the switch with other system components. The approach also needs to detect failure modes of interest to the power electronics industry, e.g., lower efficiency from an increase in on-resistance [7]. It also needs to consider the limitations and strengths of classes of boards and hardware in conducting the stress-testing needed. Finally, the approach needs to assure broad coverage, so as not to introduce unnecessary burden on the industry.

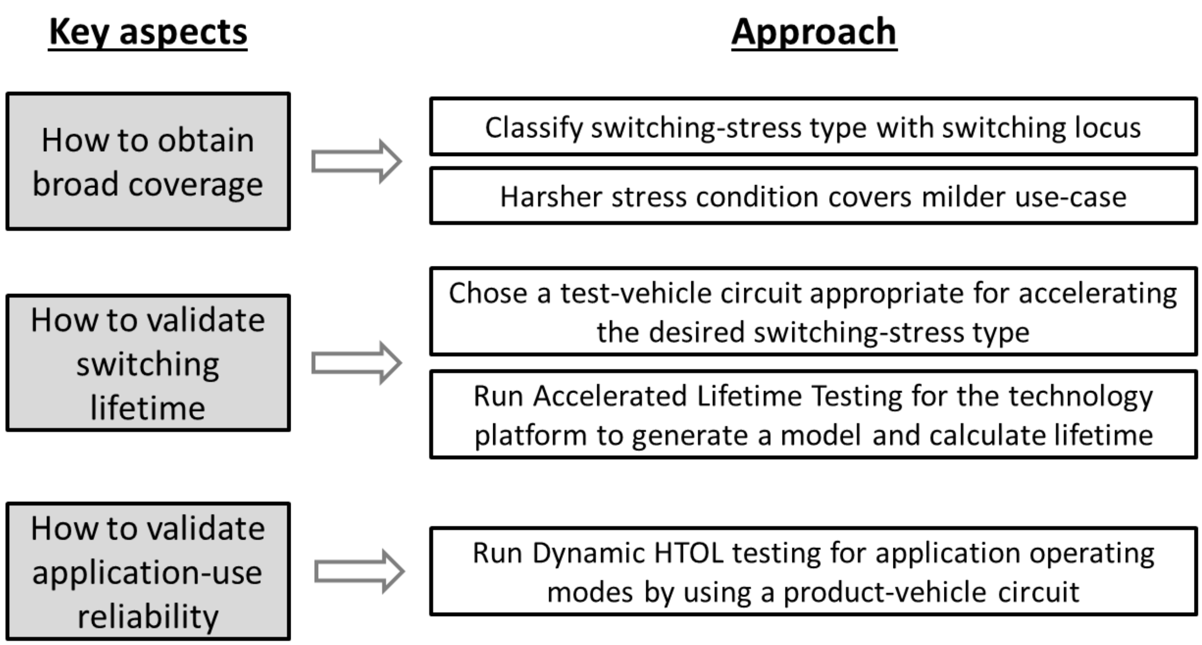

Figure 1 — Simplified explanation of the approach for assuring GaN product reliability. It consists of three key aspects as shown. The approach is not intended to be restrictive, as is described in the text.

Introduction (cont'd)

This document provides a common approach for assuring that GaN products are reliable in power conversion applications. It provides guidelines for broad coverage, addresses the detection of relevant failure modes, provides guideline stress-test procedures, and proposes common ways to collect and present data. The approach is broken down into guidelines for the three key aspects as shown in Figure 1.

1. A procedure for obtaining broad coverage by classifying the switching stress stimuli with their switching loci and explaining the use of a harsher stress condition to cover a milder use-case condition.
2. A procedure for obtaining the switching lifetime of the technology platform. This involves performing accelerated life testing with a suitable type of GaN die or core switch to generate a model.
3. A procedure for validating reliable operation under application-use conditions by running parts in an application environment using stress conditions that, if passing, would assure reliable operation for a broad range of use-conditions.

The approach is not intended to be restrictive. It takes into account the strengths and limitations of boards, hardware, and components, while also recognizing the need to not introduce unnecessary burden on the industry. It does not restrict additional testing, larger sample sizes, and stress conditions with higher acceleration. It also does not restrict the use of boards and device types. For instance, lifetime determination may be made using more complex boards or GaN switches by verifying that the complexity does not mask the acceleration of relevant failure mechanisms. Conversely simpler boards may be used to assure application-use reliability by providing collateral material showing robustness to operating modes not tested.

The core of this guideline is organized into four clauses, with clauses 5-7 reflective of the aspects of Figure 1.

- Clause 4 gives general guidance for selecting test devices, test circuits and developing test plans.
- Clause 5 provides an approach for broad coverage by using the switching locus curve.
- Clause 6 gives the procedure for obtaining wearout models and device lifetime.
- Finally, clause 7 provides guidance on validating reliable operation of GaN switches in power conversion applications.

GUIDELINE FOR SWITCHING RELIABILITY EVALUATION PROCEDURES FOR GALLIUM NITRIDE POWER CONVERSION DEVICES

(From JEDEC Board Ballot, JCB-20-06, formulated under the cognizance of the JC-70.1 subcommittee on GaN Power Electronic Conversion Semiconductor Standards.)

1 Scope

This publication presents guidelines for evaluating the switching reliability of GaN power switches. It is applicable to planar enhancement-mode, depletion-mode, GaN integrated power solutions and cascode GaN power switches. It covers the following aspects:

a) An approach for broad coverage, using the switching locus to represent switching stress in a standardized manner.

b) The development of a lifetime model, based upon the type of application switching locus.

c) The validation of reliable operation under application-use conditions.

The publication will result in common methods for representing, evaluating and modeling the switching stress on GaN power switches, and ensuring their reliable operation in an application.

2 Normative references

JEDEC JEP173, *Dynamic ON-Resistance Test Method Guidelines for GaN HEMT based Power Conversion Devices, Version 1.0*, January 2019