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EXpanded Serial Peripheral Interface (xSPI) for Non Volatile Memory Devices, Version 1.0

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EXPANDED SERIAL PERIPHERAL INTERFACE (xSPI) FOR NON VOLATILE MEMORY DEVICES

Contents

Foreword

This standard is intended for use by SoC, ASIC, ASSP, and FPGA developers or vendors interested in incorporating a master interface having a low signal count and high data transfer bandwidth with access to multiple sources of slave devices compliant with the interface. It is also, intended for use by peripheral developers or vendors interested in providing slave devices compliant with the standard, including non-volatile memories, volatile memories, graphics peripherals, networking peripherals, FPGAs, sensors, etc.

This document was prepared by the JC-42.4_3 Serial Flash task group authorized by the JC-42.4 Non-Volatile Memory subcommittee.

Introduction

This standard defines a low signal count master-slave interface for high speed byte or word serial communication with peripheral devices.

The standard defines commands for general purpose read and write of any type of peripheral device and specific commands for non-volatile memory device functions. The standard includes limited hardware and software backward compatibility with Serial Peripheral Interface (SPI) master controllers widely used in the electronics industry.

Electrical DC and AC characteristics are defined for operation with a 3 V, 1.8 V, or 1.2 V power supply.

Signaling protocols are defined for command and data transfers widths of 1, or 8 bits using either Single Data Rate (SDR) or Double Data Rate (DDR) transfers at up to 200 MHz with up to 400 MT/s.

Also, defined is a Fine-pitch Ball Grid Array (FBGA) footprint with package outline options compliant with JEDEC Publication No. 95 (JEP95), MO-234.

The purpose of this specification is to define a minimum set of requirements for JEDEC standard compliance. There are a number of existing devices that may contain legacy and/or unique manufacturer's functions in addition to the minimum JEDEC requirements. Some of these functions are defined in this document as optional operations.

EXPANDED SERIAL PERIPHERAL INTERFACE (XSPI) FOR NON VOLATILE MEMORY DEVICES

(From JEDEC Board Ballot JCB-17-29 and JCB-20-02, formulated under the cognizance of the JC-42.4 Subcommittee on Non-Volatile Memory Devices.)

1 Scope

This standard specifies the eXpanded Serial Peripheral Interface (xSPI) for Non Volatile Memory Devices, which provides high data throughput, low signal count, and limited backward compatibility with legacy Serial Peripheral Interface (SPI) devices. It is primarily for use in computing, automotive, Internet Of Things (IOT), embedded systems and mobile systems, between host processing and peripheral devices. The xSPI electrical interface can deliver up to 400 MBytes per second raw data throughput.

2 Normative Reference

The following normative documents contain provisions that through reference in this text, constitutes provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated. For undated references, the latest edition of the normative document referred to applies.

JEDEC Manual, JM7.01, *Style Manual for Standards and Other Publications of JEDEC.*

JEDEC Standard, JESD88E, *Dictionary of Terms for Solid-State Technology.*

JEDEC Standard, JESD99C, *Terms, Definitions, and Letter Symbols for Microelectronic Devices.*

JEDEC Standard, JESD100B.01, *Terms, Definitions, and Letter Symbols For Microcomputers, Microprocessors, and Memory Integrated Circuits.*

JEDEC Publication No. 95, MO-234, *Low Profile Rectangular Ball Grid Array Family, 6.00 x 8.00 x 1.20 or 1.00 mm, 24 ball package.*

JEDEC Standard, JESD8-26, *1.2 V High-Speed LVCMOS (HS_LVCMOS) Interface.*

JEDEC Standard, JESD8-31, *1.8 V High-Speed LVCMOS (HS_LVCMOS) Interface.*

JEDEC Standard, JESD8-xx, *3 V High-Speed LVCMOS (HS_LVCMOS) Interface. (In progress)*

JEDEC Standard, JESD216, *Serial Flash Discoverable Parameters (SFDP).*

JEDEC Standard, JESD252, *Serial Flash Reset Signaling Protocol.*

JEDEC Standard, JESD84-B51, *eMMC HS400 mode.*