JEDEC STANDARD

High Bandwidth Memory DRAM (HBM1, HBM2)

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Contents

Contents (cont'd)

Contents (cont'd)

HIGH BANDWIDTH MEMORY (HBM) DRAM

(From JEDEC Board Ballot JCB-19-28, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories, under item number 1797.99K, Rev. 3.30).

1 Scope

The HBM DRAM is tightly coupled to the host compute die with a distributed interface. The interface is divided into independent channels. Each channel is completely independent of one another. Channels are not necessarily synchronous to each other. The HBM DRAM uses a wide-interface architecture to achieve high-speed, low power operation. Each channel interface maintains a 128 bit data bus operating at double data rate (DDR).

2 Features

- 256 bit prefetch per memory read and write access
- BL = 2 and 4
- 128 DQ width + optional ECC pin support/channel
- Legacy mode and Pseudo Channel (PC) mode operation; 64 DQ width for PC mode
- Differential clock inputs (CK_t/CK_c) for command/address
- Double data rate (DDR) command/address. Row Activate commands require two cycles, all other commands require one cycle
- Semi-independent row and column command interfaces allowing Activates/Precharges to be issued in parallel with Read/Writes.
- Data referenced to unidirectional differential data strobes RDQS_t/RDQS_c and WDQS_t/WDQS_c. One strobe pair each per DWORD
- Up to 8 channels / device
- Channel density of 1 Gb to 16 Gb
- 8, 16, 32 or 48 banks per channel; varies by device density/channel
- Bank grouping supported
- 2 KB page size per channel
- DBIac support configurable via MRS
- Data mask for masking write data per byte
- Self refresh modes
- I/O voltage 1.2 V
- DRAM core voltage 1.2 V, independent of I/O voltage
- Unterminated data/address/cmd/clk interfaces
- Temperature sensor with 3-bit encoded range output