JEDEC STANDARD

DDR4 NVDIMM-P Bus Protocol

JESD304-4

OCTOBER 2020

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Published by
©JEDEC Solid State Technology Association 2020
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2108

PRICE: Contact JEDEC

Printed in the U.S.A.

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(From JEDEC Board Ballot, JCB-20-26, formulated under the cognizance of the JC-45.6 Subcommittee on Hybrid Modules.)

1. Scope

An NVDIMM-P device is defined as a LRDIMM memory module which provides host controller access to DRAM and/or other memory devices such as persistent memory. In order to enable access to media that may have non-deterministic access latencies, and/or on-board media management activities, which may temporarily delay access to non-volatile memory media, a handshake protocol is required to inform the host controller of availability/unavailability of return data from the DIMM. To mitigate the performance impact of this non-determinism, capabilities to enable out-of-order data transactions and to stack commands for enhanced data bus utilization are also required. A transactional protocol is described herein for NVDIMM-P, which may be used on a DDR interface allowing operation of both standard DRAM modules and NVDIMM-P modules on the same channel.

NVDIMM-P modules follow the DDR4 LRDIMM specification in pinout, electrical topology and behavior except as noted in this specification.

Minimal changes to the host controller can enable these technologies while allowing flexibility to optimize memory system performance. Options to simplify the protocol or implementation (at the expense of performance) are provided.

1.1 Reference Material

This NVDIMM-P protocol spec is a companion to the JEDEC DDR4 DRAM Standard, *JESD79-4B*, as well as the JEDEC DDR4 RCD/DB Standard and JEDEC DDR4 LRDIMM Common Standard.

2. Architecture and Initialization

2.1 NVDIMM-P bus architecture

Figure 1a shows an NVDIMM-P bus architecture example.

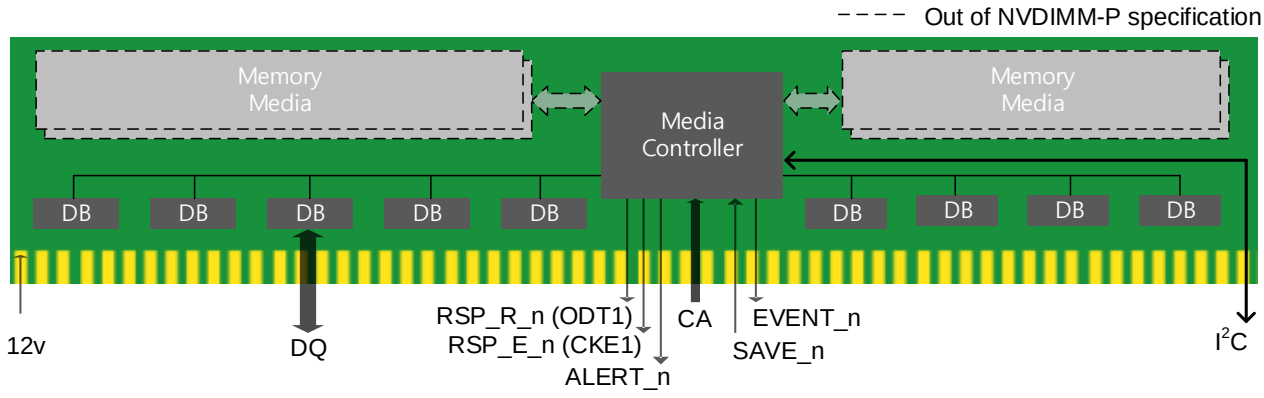

Figure 1a — Example of NVDIMM-P bus architecture