

JEDEC STANDARD

DDR4 NVDIMM-P Bus Protocol

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DDR4 NVDIMM-P BUS PROTOCOL

Contents

1.	Scope.....	1
1.1	Reference Material.....	1
2.	Architecture and Initialization	1
2.1	NVDIMM-P bus architecture.....	1
2.1.1	CA and Data bus	2
2.1.2	Response Signal.....	2
2.1.3	Event_n and Save_n.....	4
2.1.4	I2C bus	4
2.2	Data packet format.....	4
2.2.1	Read ID	6
2.2.2	Poison and User-defined metadata.....	6
2.2.3	Data Valid (D_VALID)	6
2.2.4	Write Credit (WC) and PWRITE Credit (PWC).....	6
2.3	Message packet format	8
3.	Mode control and Status Register	10
3.1	Mode Register.....	11
3.2	Media controller Control Word.....	19
3.3	Module Management Register	63
4.	Command and Operation	64
4.1	Command Truth Table	64
4.1.1	Addressability	65
4.1.2	RID	65
4.1.3	WGID	65
4.1.4	Persist	65
4.1.5	FL and Final.....	65
4.1.6	IOP Time Shift (TS) and Time Unit (TU).....	66
4.2	CKE Truth Table	66
4.3	Read Operation	67
4.3.1	XREAD and SEND	67
4.3.2	SREAD	68
4.4	Write Operation.....	69
4.4.1	XWRITE	69
4.4.2	PWRITE	70
4.5	FLUSH.....	70
4.6	Status register Read operation (READ_STATUS).....	72
4.6.1	Complete the power-up initialization.....	72
4.6.2	Available Credit Synchronization	73
4.6.3	Reset RID	73
4.7	Internal Operation (IOP).....	75
4.7.1	IOP Request	75
4.7.2	IOP0 Mode	75
4.7.3	IOP1 Mode 1.....	76
4.7.4	IOP Time	76
4.8	UNMAP.....	77
5.	DDR interface and Training.....	78
5.1	Command ordering	78
5.1.1	Read and Write Commands Ordering Rules	78
5.1.2	Flush and Write(PWRITE and XWRITE) Commands Ordering Rules	79
5.2	Data and Metadata burst ordering.....	80
5.2.1	Data Burst Ordering Rule	80

5.2.2	Metadata Burst Ordering Rule	80
5.3	DLL on/off mode and switching procedure	81
5.4	Input Clock Frequency Change.....	81
5.5	Dual Frequency Mode.....	81
5.6	Write Leveling	81
5.7	Multi-Purpose Register	81
5.8	ZQ Calibration Commands	81
5.9	DQ Vref Training	82
5.10	Command Address Parity (CA Parity)	82
5.11	Programmable Preamble & Postamble	82
5.12	Programmable Command Delay	82
5.13	DQ Training	84
5.13.1	MPR Pattern Mode	84
5.13.2	Advanced FIFO Training Mode.....	84
5.13.3	Data Buffer Training	85
5.14	Unsupported DDR functions.....	86
6.	Functional Features	87
6.1	Read/Write buffer management	87
6.1.1	Read buffer management	87
6.1.2	Write buffer management	87
6.2	All-Zeros Fail-Prevention Mode.....	89
6.3	Write Data grouping.....	89
6.4	Data Persistence in the Event of a Power Loss	92
7.	Error and Event Alert	94
7.1	Error type	94
7.1.1	CA parity error	94
7.1.2	Read Channel error	94
7.1.3	Write Channel error	94
7.1.4	UE response of read request	95
7.1.5	Interrupt	95
7.1.6	Urgent error	96
7.1.7	Data persistency error in the event of a Power Loss	97
7.2	Error handling and recovery	97
7.3	Error Injection.....	98
8.	Power Management	99
8.1	Power-up and Reset initialization	99
8.1.1	Power-up initialization	99
8.1.2	Reset initialization	101
8.2	Power saving mode	101
8.2.1	Non-clock Stopped Power-down	101
8.2.2	Clock Stopped Power-down.....	103
8.2.3	Self-Refresh	104
9.	Channel Error Correction Code (ECC)	106
9.1.1	Data Mapping	106
9.1.2	Field Definition	108
9.1.3	Generator Polynomial	109
10.	On-Die Termination	110
11.	Absolute Maximum Ratings	110
12.	AC & DC Input/Output Measurement Levels	110
13.	Speed Bin.....	110
14.	Input/Output Capacitance	113
15.	Electrical Characteristics and AC Timing	113

Figures

Figure 1 - Response Signaling	3
Figure 2. NVDIMM-P XREAD Operation	67
Figure 3. Back-to-back NVDIMM-P XREAD Operations	67
Figure 4. NVDIMM-P XREAD operation with minimum tRRSE timing value	68
Figure 5. NVDIMM-P SREAD Operation	68
Figure 6. NVDIMM-P XWRITE Operation	69
Figure 7. Back-to-back NVDIMM-P XWRITE Operation.....	69
Figure 8. NVDIMM-P PWRITE Operation.....	70
Figure 9. The FLUSH command and completion response by W_PER.	71
Figure 10. READ_STATUS Operation.....	72
Figure 11. NVDMM-P Reset RID operation	73
Figure 12. Multiple Reset RID commands with single RD_RDY response case 1	74
Figure 13. Multiple Reset RID commands with additional RD_RDY response case 2	74
Figure 14. Multiple Reset RID commands with additional RD_RDY response case 3	74
Figure 15. NVDIMM-P IOP Mode 0 Operation	75
Figure 16. NVDIMM-P IOP Mode 1 Operation	76
Figure 17. RAW timing diagram	78
Figure 18. WAR timing diagram.....	78
Figure 19. Delay elements for reads and writes.....	82
Figure 20. Delay added for Data Buffer DB-A.....	83
Figure 21. Advanced FIFO Training Example.....	85
Figure 22. Write buffer implementations	88
Figure 23. MRACT-WGID and SEND-MRR timing	90
Figure 24. WGID bitmap status flow.....	91
Figure 25. WGID bitmap status flow with uncorrectable channel error	92
Figure 26: Write channel ECC Error Reporting	94
Figure 27: NVDMM-P Interrupt message operation	95
Figure 28. NVDIMM-P Power-up Sequence.....	101
Figure 29. NVDIMM-P Power-Down Entry	101
Figure 30. NVDIMM-P CKE Power-Down Exit with Response Signal & SEND Examples	102
Figure 31. MRs Use in Clock Stopped Power-Down Entry	103
Figure 32. Clock Stopped Power-Down Exit with Response Signal & SEND Examples	104
Figure 33. Self-Refresh Entry/Exit Timing.....	105
Figure 34. NVDIMM-P ECC Data Mapping.....	106

Tables

Table 1 - Response Signal Pin Assignment.....	2
Table 2 - Response Signal Encoding	3
Table 3 - Write data packet format for XWRITE and PWRITE	4
Table 4 - Read data and message packet format for SEND	4
Table 5 - Read data packet format for SREAD.....	5
Table 6 - Write data packet format for XWRITE and PWRITE	5
Table 7 - Read data and message packet format for SEND	5
Table 8 - Read data packet format for SREAD.....	5
Table 9 - Write Credit Return	7
Table 10 - Poison and PWRITE Credit return	7
Table 11 - Credit Return with CTH	8
Table 12 - NVDIMM-P Message Packet Format.....	9
Table 13 –NVDIMM-P special function registers	10
Table 14 - Write data Recovery time (cycles).....	11
Table 15 - CAS Latency	12
Table 16 - Output Driver Impedance Control	13
Table 17 - CAS Write Latency (CWL)	14
Table 18 - MPR Data Format with MPR page 0 (Training Pattern)	16
Table 19. MPR Data Format with MPR page 2 (MPR Readout).....	16
Table 20. MPR Data Format with MPR page 3 (Vendor use only) ¹	16
Table 21. RTT_PARK.....	18
Table 22. tDLLK.....	19
Table 23. Function Space 0.....	20
Table 24. Function Space 1	21
Table 25. Function Space 2.....	22
Table 26. Function Space 3.....	23
Table 27. Function Space 4.....	23
Table 28. Function Space 7.....	24
Table 29 - F0RC02: Timing and IBT Control Word	24
Table 30 - F0RC06: Command Space Control Word definition	25
Table 31 - F0RC09: Power Saving Settings Control Word.....	26
Table 32 - F0RC0A: NVDIMM Operating Speed ¹	26
Table 33 - F0RC0B: Operating Voltage VDD and VrefCA Source Control Word.....	27
Table 34 - F0RC0C: Training Control Word.....	27
Table 35 - F0RC0D: DIMM Configuration Control Word	28
Table 36 - F0RC0E: Parity and ALERT Configuration Control Word	28
Table 37 - F0RC0F: Command Latency Adder Control Word	29
Table 38 - F0RC1x: Internal VrefCA Control Word	29
Table 39 - F0RC2x: I ² C Bus Control Word	31
Table 40 - F0RC3x: Fine Granularity NVDIMM Operating Speed ¹	32
Table 41 - F0RC4x: CW Source Selection Control Word.....	36
Table 42 -. F0RC5x: CW Destination Selection & Write/Read Additional QxODT[1:0] Signal High	36
Table 43 - F0RC6x: CW Data Control Word.....	37

Table 44. F0RC7x: IBT Control Word.....	37
Table 45. F0RC8x: ODT Input Buffer/IBT, QxODT Output Buffer and Timing Control Word.....	38
Table 46. F0RCBx: IBT and MRS Snoop	39
Table 47. F0RCCx~ F0RCFx: CA Parity Error Log.....	40
Table 48. F1RC00: Data Buffer Interface Driver Characteristics Control Word	40
Table 49. F1RC05: Data Buffer Interface Output Slew Rate Control	41
Table 50. F1RC8x: BCOM[3:0]/BCKE/BODT Output Delay Control Word.....	41
Table 51. F1RC9x: BCK Output Delay Control Word	42
Table 52. F2RC03: NVDIMM-P controller status.....	42
Table 53. F2RC3x: Power Saving Modes.....	43
Table 54. F2RC4x: Packet and timing option control.....	43
Table 55. F2RC5x: Correctable Channel Error Interrupt Threshold and Enable	43
Table 56. F2RC6x: Error Injection–Enable, Type	44
Table 57. F2RC7x: Error Injection –Error Address0	44
Table 58. F2RC7x: Error Injection – Error Mask0	45
Table 59. F2RC8x: Error Injection – Error Address1	45
Table 60. F2RC8x: Error Injection – Error Mask1	45
Table 61. F2RC9x: Error Injection – Error Address2	45
Table 62. F2RC9x: Error Injection – Error Mask2	46
Table 63. F2RCAx: Error Injection – Error Address3	46
Table 64. F2RCAx: Error Injection – Error Mask3	46
Table 65. F2RCBx: Error Injection – Error Address4	46
Table 66. F2RCBx: Error Injection – Error Mask4	47
Table 67. F2RCCx: Urgent Error Log – Urgent Write Error	47
Table 68. F2RCDx: Urgent Error Log – Urgent Read Error.....	47
Table 69. F2RCEx: Urgent Error Log – Error RID	47
Table 70. F2RCFx: Urgent Error Log – Urgent Controller Error	47
Table 71. F3RC00: Programmable READ command delay Control Word.....	48
Table 72. F3RC01: Programmable WRITE command delay Control Word.....	48
Table 73. F3RC08, F3RC09: VrefDQ Training for DQ0~3 Control Word	48
Table 74. VrefDQ Training: Value	49
Table 75. F3RC0A, F3RC0B: VrefDQ Training for DQ4~7 Control Word	50
Table 76. F3RC0C, F3RC0D: VrefDQ Training for DQ8~11 Control Word.....	50
Table 77. F3RC0E, F3RC0F: VrefDQ Training for DQ12~15 Control Word	51
Table 78. F3RC1x: VrefDQ Training for DQ16~19 Control Word	51
Table 79. F3RC2x: VrefDQ Training for DQ20~23 Control Word	52
Table 80. F3RC3x: VrefDQ Training for DQ24~27 Control Word	52
Table 81. F3RC4x: VrefDQ Training for DQ28~31 Control Word	52
Table 82. F3RC5x: VrefDQ Training for DQ32~35 Control Word	53
Table 83. F3RC6x: VrefDQ Training for DQ36~39 Control Word	53
Table 84. F3RC7x: VrefDQ Training for DQ40~43 Control Word	53
Table 85. F3RC8x: VrefDQ Training for DQ44~47 Control Word	54
Table 86. F3RC9x: VrefDQ Training for DQ48~51 Control Word	54
Table 87. F3RCAx: VrefDQ Training for DQ52~55 Control Word	54

Table 88. F3RCBx: VrefDQ Training for DQ56~59 Control Word.....	55
Table 89. F3RCCx: VrefDQ Training for DQ60~63 Control Word.....	55
Table 90. F3RCDx: VrefDQ Training for CB0~3 Control Word.....	55
Table 91. F3RCEx: VrefDQ Training for CB4~7 Control Word	56
Table 92. F4RC8x~F4RCEx: Event Log	56
Table 93. F7RC1x: Date Code Byte 0	57
Table 94. F7RC2x: Date Code Byte 1	58
Table 95. F7RC3x: Date Code Byte 2	59
Table 96. F7RC4x: Vendor Specific Unique Unit Code Byte 0.....	59
Table 97. F7RC5x: Vendor Specific Unique Unit Code Byte 1.....	60
Table 98. F7RC6x: Vendor Specific Unique Unit Code Byte 2.....	60
Table 99. F7RC7x: Vendor Specific Unique Unit Code Byte 3.....	60
Table 100. F7RC8x: Vendor Specific Unique Unit Code Byte 4.....	61
Table 101. F7RC9x: Vendor Specific Unique Unit Code Byte 5.....	61
Table 102. F7RCAx: Vendor Specific Unique Unit Code Byte 6.....	61
Table 103. F7RCBx: Vendor ID Byte 0 ¹	62
Table 104. F7RCCx: Vendor ID Byte 1 ¹	62
Table 105. F7RCDx: Device ID Byte 0 ¹	62
Table 106. F7RCEx: Device ID Byte 1 ¹	63
Table 107. F7RCFx: Revision ID ¹	63
Table 108. NVDIMM-P Command Truth Table	64
Table 109. FLUSH command modes.....	70
Table 110. READ_STATUS command encoding	72
Table 111. IOP Shift Time Definition	76
Table 112. Minimum IOP Time Intervals	76
Table 113. IOP Time Intervals and Ranges for DDR4-3200.....	77
Table 114. Definition of OPCODE for UNMAP.....	77
Table 115. Burst Order by XREAD ADDR[2]	80
Table 116 –Option-A format example by MCW F2RC4x DA[0] setting	81
Table 117. Example of Case 1	88
Table 118. Example of Case 2	89
Table 119. WGID bitmap format	90
Table 120. Final Flush Modes	93
Table 121. Interrupt type.....	96
Table 122. Interrupt Status.....	96
Table 123. Self-Refresh mode	105
Table 124. NVDIMM-P ECC Data Mapping	107
Table 125. Primitive Polynomial Matrix	108
Table 126. Generator Polynomial Matrix (Hex values).....	109
Table 127. Timing parameter	110
Table 128. Timing parameter by Speed Grade.....	112

DDR4 NVDIMM-P BUS PROTOCOL

(From JEDEC Board Ballot, JCB-20-26, formulated under the cognizance of the JC-45.6 Subcommittee on Hybrid Modules.)

1. Scope

An NVDIMM-P device is defined as a LRDIMM memory module which provides host controller access to DRAM and/or other memory devices such as persistent memory. In order to enable access to media that may have non-deterministic access latencies, and/or on-board media management activities, which may temporarily delay access to non-volatile memory media, a handshake protocol is required to inform the host controller of availability/unavailability of return data from the DIMM. To mitigate the performance impact of this non-determinism, capabilities to enable out-of-order data transactions and to stack commands for enhanced data bus utilization are also required. A transactional protocol is described herein for NVDIMM-P, which may be used on a DDR interface allowing operation of both standard DRAM modules and NVDIMM-P modules on the same channel.

NVDIMM-P modules follow the DDR4 LRDIMM specification in pinout, electrical topology and behavior except as noted in this specification.

Minimal changes to the host controller can enable these technologies while allowing flexibility to optimize memory system performance. Options to simplify the protocol or implementation (at the expense of performance) are provided.

1.1 Reference Material

This NVDIMM-P protocol spec is a companion to the JEDEC DDR4 DRAM Standard, *JESD79-4B*, as well as the JEDEC DDR4 RCD/DB Standard and JEDEC DDR4 LRDIMM Common Standard.

2. Architecture and Initialization

2.1 NVDIMM-P bus architecture

Figure 1a shows an NVDIMM-P bus architecture example.

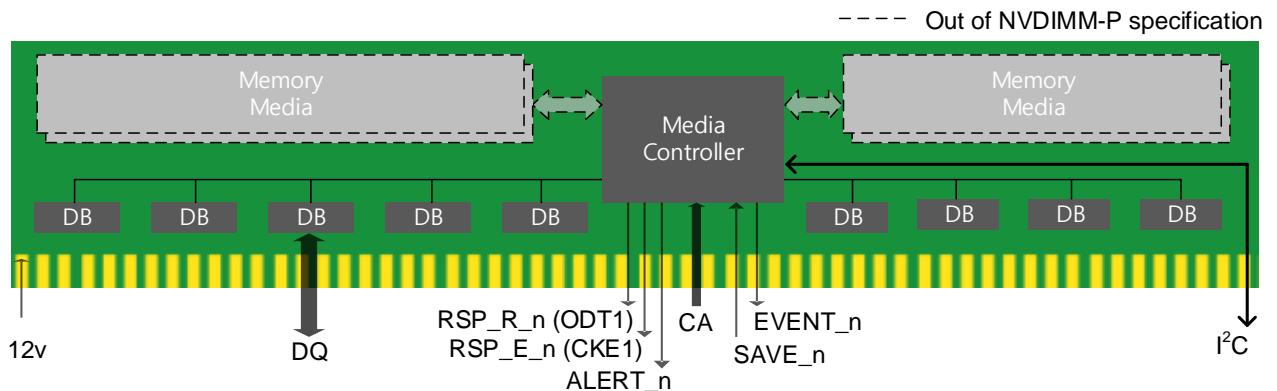


Figure 1a — Example of NVDIMM-P bus architecture