

JEDEC STANDARD

Serial Flash Discoverable Parameters (SFDP)

JESD216F

(Revision of JESD216E, September 2021)

DECEMBER 2021

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2021
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2108

JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

This page left intentionally blank

Contents

		Page
	Foreword	x
	Introduction.....	x
1	Scope.....	1
2	Normative reference.....	1
3	Terms and definitions	2
4	Read SFDP Command Protocol.....	3
4.1	Instruction	3
4.2	Address	3
4.3	Wait States	4
4.4	Clock Rate.....	4
4.5	Command Modes	4
4.5.1	Read SFDP (1S-1S-1S) Mode	5
4.5.2	Read SFDP (2S-2S-2S) Mode	6
4.5.3	Read SFDP (4S-4S-4S) Mode	6
4.5.4	Read SFDP (4S-4D-4D) Mode	7
4.5.5	Read SFDP (8D-8D-8D) Mode	7
4.5.6	Fetch SFDP (1S-1S-1S) Mode.....	8
4.5.7	Fetch SFDP (2S-2S-2S) Mode.....	8
4.5.8	Fetch SFDP (4S-4S-4S and 4S-4D-4D) Mode	9
4.5.9	Fetch SFDP (8D-8D-8D) Mode.....	9
5	Read SFDP Behavior	10
5.1	Security	10
5.2	Reset and Hold Functions	10
5.3	Read Wrap	10
5.4	SFDP Address Boundary Wrap	10
5.5	Reserved SFDP Locations	10
6	SFDP Database	11
6.1	SFDP Header Structure.....	11
6.2	SFDP Header	12
6.2.1	SFDP Header: 1 st DWORD.....	12
6.2.2	SFDP Header: 2 nd DWORD.....	13
6.2.3	Definition of SFDP Access Protocol Field	14
6.3	Parameter Headers	19

6.3.1	Parameter Header: 1 st DWORD	19
6.3.2	Parameter Header: 2 nd DWORD	20
6.3.3	Definition of Parameter ID Field	20
6.3.4	Example SFDP Headers.....	21
6.4	JEDEC Basic Flash Parameter Header and Table	24
6.4.1	JEDEC Basic Flash Parameter Header: 1st DWORD	24
6.4.2	JEDEC Basic Flash Parameter Header: 2nd DWORD	25
6.4.3	JEDEC Basic Flash Parameter Table Overview	25
6.4.4	JEDEC Basic Flash Parameter Table: 1 st DWORD	26
6.4.5	JEDEC Basic Flash Parameter Table: 2 nd DWORD	28
6.4.6	JEDEC Basic Flash Parameter Table: 3 rd DWORD	28
6.4.7	JEDEC Basic Flash Parameter Table: 4 th DWORD.....	29
6.4.8	JEDEC Basic Flash Parameter Table: 5 th DWORD.....	30
6.4.9	JEDEC Basic Flash Parameter Table: 6 th DWORD.....	30
6.4.10	JEDEC Basic Flash Parameter Table: 7 th DWORD.....	31
6.4.11	JEDEC Basic Flash Parameter Table: 8 th DWORD.....	31
6.4.12	JEDEC Basic Flash Parameter Table: 9 th DWORD.....	32
6.4.13	JEDEC Basic Flash Parameter Table: 10 th DWORD.....	32
6.4.14	JEDEC Basic Flash Parameter Table: 11 th DWORD.....	34
6.4.15	JEDEC Basic Flash Parameter Table: 12 th DWORD.....	36
6.4.16	JEDEC Basic Flash Parameter Table: 13 th DWORD.....	38
6.4.17	JEDEC Basic Flash Parameter Table: 14 th DWORD.....	39
6.4.18	JEDEC Basic Flash Parameter Table: 15 th DWORD.....	40
6.4.19	JEDEC Basic Flash Parameter Table: 16 th DWORD.....	42
6.4.20	JEDEC Basic Flash Parameter Table: 17 th DWORD.....	44
6.4.21	JEDEC Basic Flash Parameter Table: 18 th DWORD.....	45
6.4.22	JEDEC Basic Flash Parameter Table: 19 th DWORD.....	48
6.4.23	JEDEC Basic Flash Parameter Table: 20 th DWORD.....	49
6.4.24	JEDEC Basic Flash Parameter Table: 21 st DWORD	52
6.4.25	JEDEC Basic Flash Parameter Table: 22 nd DWORD	53
6.4.26	JEDEC Basic Flash Parameter Table: 23 rd DWORD	54
6.5	JEDEC Sector Map Parameter Header and Table	55
6.5.1	Sector Map Parameter Header: 1 st DWORD	56
6.5.2	Sector Map Parameter Header: 2 nd DWORD.....	56
6.5.3	Configuration Detection Command Descriptor, 1 st DWORD	57
6.5.4	Configuration Detection Command Descriptor, 2 nd DWORD.....	58

6.5.5	Configuration Map Descriptor Header DWORD	59
6.5.6	Region DWORD.....	59
6.5.7	Sector Map Parameter Table – Example 1.....	60
6.5.8	Sector Map Parameter Table – Example 2.....	64
6.6	Replay Protected Monotonic Counters (RPMC) Parameter Header and Table	65
6.6.1	Replay Protected Monotonic Counters Parameter Header: 1 st DWORD.....	65
6.6.2	Replay Protected Monotonic Counters Parameter Header: 2 nd DWORD.....	65
6.6.3	Replay Protected Monotonic Counters Parameter Table, 1 st DWORD	66
6.6.4	Replay Protected Monotonic Counters Parameter Table, 2 nd DWORD	67
6.7	JEDEC 4-byte Address Instruction Parameter Header and Table	67
6.7.1	4-byte Address Instruction Parameter Header: 1 st DWORD	68
6.7.2	4-byte Address Instruction Parameter Header: 2 nd DWORD.....	68
6.7.3	4-byte Address Instruction Table, 1 st DWORD	69
6.7.4	4-byte Address Instruction Table, 2 nd DWORD	71
6.8	JEDEC eXtended Serial Peripheral Interface (xSPI) Profile 1.0 Parameter Header and Table.....	72
6.8.1	JEDEC xSPI (Profile 1.0) Parameter Header: 1 st DWORD.....	72
6.8.2	JEDEC xSPI (Profile 1.0) Parameter Header: 2 nd DWORD.....	72
6.8.3	JEDEC xSPI (Profile 1.0) Parameter Table: 1 st DWORD - Command Codes used in 8D-8D-8D protocol mode	73
6.8.4	JEDEC xSPI (Profile 1.0) Parameter Table: 2 nd DWORD - Command Codes used in 8D-8D-8D protocol mode	74
6.8.5	JEDEC xSPI (Profile 1.0) Parameter Table: 3 rd DWORD - Memory Commands Supported in 8D-8D-8D protocol mode	74
6.8.6	JEDEC xSPI (Profile 1.0) Parameter Table: 4 th DWORD - Dummy cycles used for various frequencies.....	76
6.8.7	JEDEC xSPI (Profile 1.0) Parameter Table: 5 th DWORD - Dummy cycles used for various frequencies.....	76
6.8.8	JEDEC xSPI (Profile 1.0) Parameter Table: 6 th DWORD – Default Dummy cycles after POR... ..	76
6.9	JEDEC eXtended Serial Peripheral Interface (xSPI) - Profile 2.0 Parameter Header and Table ..	77
6.9.1	JEDEC xSPI (Profile 2.0) Parameter Header: 1 st DWORD.....	77
6.9.2	JEDEC xSPI (Profile 2.0) Parameter Header: 2 nd DWORD.....	77
6.9.3	JEDEC xSPI (Profile 2.0) Parameter Table: 1 st DWORD - Command Codes used in 8D-8D-8D Profile 2.0 protocol mode	78
6.9.4	JEDEC xSPI (Profile 2.0) Parameter Table: 2 nd DWORD - Dummy cycles used for various frequencies.....	80
6.9.5	JEDEC xSPI (Profile 2.0) Parameter Table: 3 rd DWORD - Dummy cycles used for various frequencies.....	80
6.10	Status, Control and Configuration Register Map for SPI Memory Devices	80
6.10.1	SCCR Map for SPI Memory Devices Parameter Header: 1 st DWORD	82

6.10.2	SCCR Map for SPI Memory Devices Parameter Header: 2 nd DWORD.....	82
6.10.3	SCCR Map for SPI Memory Devices Parameter Table: 1 st DWORD – Volatile registers address offset	82
6.10.4	SCCR Map for SPI Memory Devices Parameter Table: 2 nd DWORD – Non-Volatile registers address offset	82
6.10.5	SCCR Map for SPI Memory Devices Parameter Table: 3 rd DWORD – Generic Addressable Read/Write Status/Control register commands for volatile registers.....	83
6.10.6	SCCR Map for SPI Memory Devices Parameter Table: 4 th DWORD – Generic Addressable Read/Write Status/Control register commands for non-volatile registers	84
6.10.7	SCCR Map for SPI Memory Devices Parameter Table: 5 th DWORD – WIP (Required for xSPI)	85
6.10.8	SCCR Map for SPI Memory Devices Parameter Table: 6 th DWORD – WEL.....	86
6.10.9	SCCR Map for SPI Memory Devices Parameter Table: 7 th DWORD – Program Error	87
6.10.10	SCCR Map for SPI Memory Devices Parameter Table: 8 th DWORD – Erase Error	88
6.10.11	SCCR Map for SPI Memory Devices Parameter Table: 9 th DWORD – Variable Dummy Cycle Settings – Volatile Register	89
6.10.12	SCCR Map for SPI Memory Devices Parameter Table: 10 th DWORD – Variable Dummy Cycle Settings- Non Volatile Register	90
6.10.13	SCCR Map for SPI Memory Devices Parameter Table: 11 th DWORD – Variable Dummy Cycle Settings – bit patterns.....	91
6.10.14	SCCR Map for SPI Memory Devices Parameter Table: 12 th DWORD – Variable Dummy Cycle Settings – bit patterns.....	92
6.10.15	SCCR Map for SPI Memory Devices Parameter Table: 13 th DWORD – Variable Dummy Cycle Settings – bit patterns.....	93
6.10.16	SCCR Map for SPI Memory Devices Parameter Table: 14 th DWORD – QPI Mode Enable Volatile.....	94
6.10.17	SCCR Map for SPI Memory Devices Parameter Table: 15 th DWORD – QPI Mode Enable - Non Volatile.....	95
6.10.18	SCCR Map for SPI Memory Devices Parameter Table: 16 th DWORD – Octal Mode Enable – Volatile.....	96
6.10.19	SCCR Map for SPI Memory Devices Parameter Table: 17 th DWORD – Octal Mode Enable- Non-Volatile.....	97
6.10.20	SCCR Map for SPI Memory Devices Parameter Table: 18 th DWORD – STR or DTR mode select – Volatile.....	98
6.10.21	SCCR Map for SPI Memory Devices Parameter Table: 19 th DWORD – STR or DTR mode select – Non Volatile.....	99
6.10.22	SCCR Map for SPI Memory Devices Parameter Table: 20 th DWORD – STR Octal Mode Enable – Volatile.....	100
6.10.23	SCCR Map for SPI Memory Devices Parameter Table: 21 st DWORD – STR Octal Mode Enable - Non-Volatile	101
6.10.24	SCCR Map for SPI Memory Devices Parameter Table: 22 nd DWORD – DTR Octal Mode Enable – Volatile.....	102

6.10.25	SCCR Map for SPI Memory Devices Parameter Table: 23 rd DWORD – DTR Octal Mode Enable – Non-Volatile	103
6.10.26	SCCR Map for SPI Memory Devices Parameter Table: 24 th DWORD – DPD Status	104
6.10.27	SCCR Map for SPI Memory Devices Parameter Table: 25 th DWORD – UDPD Status	105
6.10.28	SCCR Map for SPI Memory Devices Parameter Table: 26 th DWORD – Output Driver Strength - Volatile.....	106
6.10.29	SCCR Map for SPI Memory Devices Parameter Table: 27 th DWORD – Output Driver Strength – Non Volatile.....	107
6.10.30	SCCR Map for SPI Memory Devices Parameter Table: 28 th DWORD – Output Driver Strength control bit patterns	108
6.11	Status, Control and Configuration Register Map for xSPI Profile 2.0 Memory Devices	109
6.11.1	SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Header: 1 st DWORD.....	110
6.11.2	SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Header: 2 nd DWORD.....	110
6.11.3	SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 1 st DWORD – Volatile registers address offset.....	110
6.11.4	SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 2 nd DWORD – Non-Volatile registers address offset.....	110
6.11.5	SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 3 rd DWORD – Generic Addressable Read/Write Status/Control register commands	111
6.11.6	SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 4 th DWORD – Program Error	112
6.11.7	SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 5 th DWORD – Erase Error	112
6.11.8	SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 6 th DWORD – Variable Dummy Cycle Settings – Volatile Register	113
6.11.9	SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 7 th DWORD – Variable Dummy Cycle Settings- Non Volatile Register	114
6.11.10	SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 8 th DWORD – Variable Dummy Cycle Settings – bit patterns	115
6.11.11	SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 9 th DWORD – Variable Dummy Cycle Settings – bit patterns	116
6.11.12	SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 10 th DWORD – Variable Dummy Cycle Settings – bit patterns	117
6.11.13	SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 11 th DWORD – Output Driver Strength - Volatile	118
6.11.14	SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 12 th DWORD – Output Driver Strength – Non Volatile.....	118
6.11.15	SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 13 th DWORD – Output Driver Strength control bit patterns	119
6.12	Status, Control and Configuration Register Map Offsets for Multi-Chip SPI Memory Devices	120
6.12.1	Status, Control and Configuration Register Map Parameter Header: 1 st DWORD	120

6.12.2	Status, Control and Configuration Register Map Parameter Header: 2 nd DWORD	120
6.12.3	Status, Control and Configuration Register Map Parameter Table: 1 st DWORD – Volatile registers address offset for die 1	121
6.12.4	Status, Control and Configuration Register Map Parameter Table: 2 nd DWORD – Non-Volatile registers address offset for die 1	121
6.12.5	Status, Control and Configuration Register Map Parameter Table: 3 rd DWORD – Volatile registers address offset for die 2	121
6.12.6	Status, Control and Configuration Register Map Parameter Table: 4 th DWORD – Non-Volatile registers address offset for die 2	121
6.12.7	Status, Control and Configuration Register Map Parameter Table: 5 th DWORD – Volatile registers address offset for die 3	121
6.12.8	Status, Control and Configuration Register Map Parameter Table: 6 th DWORD – Non-Volatile registers address offset for die 3	121
6.13	Command Sequences to Change to Octal DDR (8D-8D-8D) mode.....	122
6.13.1	Command Sequences to Change to Octal DDR (8D-8D-8D) mode, Parameter Header: 1 st DWORD	123
6.13.2	Command Sequences to Change to Octal DDR (8D-8D-8D) mode, Parameter Header: 2 nd DWORD	123
6.13.3	Command Sequences to Change to Octal DDR (8D-8D-8D) mode, Parameter Table: 1 st DWORD - First Command Sequence.....	123
6.13.4	Command Sequences to Change to Octal DDR (8D-8D-8D) mode, Parameter Table: 2 nd DWORD - First Command Sequence (continued).....	124
6.13.5	Command Sequences to Change to Octal DDR (8D-8D-8D) mode, Parameter Table: 3 rd DWORD - 2 nd Command Sequence.....	124
6.13.6	Command Sequences to Change to Octal DDR (8D-8D-8D) mode, Parameter Table: 4 th DWORD - 2 nd Command Sequence (continued)	124
6.13.7	Command Sequences to Change to Octal DDR (8D-8D-8D) mode, Parameter Table: 5 th DWORD - 3 rd Command Sequence	124
6.13.8	Command Sequences to Change to Octal DDR (8D-8D-8D) mode, Parameter Table: 6 th DWORD - 3 rd Command Sequence (continued).....	125
6.13.9	Command Sequences to Change to Octal DDR (8D-8D-8D) mode, Parameter Table: 7 th DWORD - 4 th Command Sequence	125
6.13.10	Command Sequences to Change to Octal DDR (8D-8D-8D) mode, Parameter Table: 8 th DWORD - 4 th Command Sequence (continued).....	125
6.14	x4 Quad IO with DS Parameter Header and Table.....	126
6.14.1	x4 Quad IO with DS Parameter Header: 1st DWORD	126
6.14.2	x4 Quad IO with DS Parameter Header: 2nd DWORD.....	126
6.14.3	x4 Quad IO with DS Parameter Table: 1st DWORD - Command Codes used in 4S-4D-4D protocol mode	127
6.14.4	x4 Quad IO with DS Parameter Table: 2nd DWORD - Command Codes used in 4S-4D-4D protocol mode	128

6.14.5	x4 Quad IO with DS Parameter Table: 3rd DWORD - Memory Commands Supported in 4S-4D-4D protocol mode	128
6.14.6	x4 Quad IO with DS Parameter Table: 4th DWORD - Dummy cycles used for various frequencies	129
6.14.7	x4 Quad IO with DS Parameter Table: 5th DWORD - Dummy cycles used for various frequencies	129
6.15	Command Sequences to Change to Quad DDR (4S-4D-4D) mode	130
6.15.1	Command Sequences to Change to Quad DDR (4S-4D-4D) mode, Parameter Header: 1st DWORD	131
6.15.2	Command Sequences to Change to Quad DDR (4S-4D-4D) mode, Parameter Header: 2nd DWORD	131
6.15.3	Command Sequences to Change to Quad DDR (4S-4D-4D) mode, Parameter Table: 1st DWORD - First Command Sequence	131
6.15.4	Command Sequences to Change to Quad DDR (4S-4D-4D) mode, Parameter Table: 2nd DWORD - First Command Sequence (continued)	132
6.15.5	Command Sequences to Change to Quad DDR (4S-4D-4D) mode, Parameter Table: 3rd DWORD - 2nd Command Sequence	132
6.15.6	Command Sequences to Change to Quad DDR (4S-4D-4D) mode, Parameter Table: 4th DWORD - 2nd Command Sequence (continued)	132
6.15.7	Command Sequences to Change to Quad DDR (4S-4D-4D) mode, Parameter Table: 5th DWORD - 3rd Command Sequence	132
6.15.8	Command Sequences to Change to Quad DDR (4S-4D-4D) mode, Parameter Table: 6th DWORD - 3rd Command Sequence (continued)	133
6.15.9	Command Sequences to Change to Quad DDR (4S-4D-4D) mode, Parameter Table: 7th DWORD - 4th Command Sequence	133
6.15.10	Command Sequences to Change to Quad DDR (4S-4D-4D) mode, Parameter Table: 8th DWORD - 4th Command Sequence (continued)	133
6.16	Secure Packet READ/WRITE Parameter Header and Table	133
6.16.1	Secure Packet READ/WRITE Parameter Header: 1 st DWORD	134
6.16.2	Secure Packet READ/WRITE Parameter Header: 2 nd DWORD	134
6.16.3	Secure Packet READ/WRITE Parameter Table, 1 st DWORD	135
6.16.4	Secure Packet READ/WRITE Parameter Table, 2 nd DWORD	135
6.16.5	Secure Packet READ/WRITE Parameter Table, 3 rd DWORD	135
6.16.6	Secure Packet READ/WRITE Parameter Table, 4 th DWORD	136
7	Rules for Header and Table Additions and Modifications	137
8	Legacy Compatibility	138
Annex A	- (Informative) Procedure for Requesting Function Specific ID	139
Annex B	- (Informative) Differences between revisions	140
B.1	Differences between JESD216F and JESD216E	140
B.2	Differences between JESD216E and JESD216D.01	140

B.3	Differences between JESD216D.01 and JESD216D	140
B.4	Differences between JESD216D and JESD216C	142
B.5	Differences between JESD216C and JESD216B	142
B.6	Differences between JESD216B and JESD216A	144
B.7	Differences between JESD216A and JESD216.....	145

Figures

Figure 1 — Read SFDP (1S-1S-1S) Mode Timing Diagram	5
Figure 2 — Read SFDP (2S-2S-2S) Mode Timing Diagram	6
Figure 3 — Read SFDP (4S-4S-4S) Mode Timing Diagram	6
Figure 4 — Read SFDP (4S-4D-4D) Mode Timing Diagram	7
Figure 5 — Read SFDP (8D-8D-8D) Mode Timing Diagram.....	7
Figure 6 — Fetch SFDP (1S-1S-1S) Mode Timing Diagram.....	8
Figure 7 — Fetch SFDP (2S-2S-2S) Mode Timing Diagram.....	8
Figure 8 — Fetch SFDP (4S-4S-4S and 4S-4D-4D) Mode Timing Diagram	9
Figure 9 — Fetch SFDP (8D-8D-8D) Mode Timing Diagram.....	9
Figure 10 — Overall Header Structure	11
Figure 11 — xSPI NAND Class-1 Device Read SFDP Flow.....	17
Figure 12 — xSPI NAND Class-2 Device Read SFDP Flow.....	18
Figure 13 — Example SFDP Header with single Basic Parameter Table	22
Figure 14 — Example SFDP Header with single Basic Parameter Table Word based (xSPI Profile 2.0)	22
Figure 15 — Example SFDP Header with two Basic parameter Tables	23
Figure 16 — Example SFDP Header with two basic Parameter Tables and one optional (4-Byte Address) Function Specific Tables	23
Figure 17 — Example SFDP Header with two basic Parameter Tables and two optional (4-Byte Address and Status, Control and Configuration Register Map) Function Specific Tables	24
Figure 18 — Data Strobe Waveforms in STR Mode – Option 11b.....	46
Figure 19 — Data Strobe Waveforms in STR Mode - Option 10b.....	46
Figure 20 — Data Strobe Waveforms in STR Mode - Option 01b.....	47

Foreword

This standard was prepared by the JEDEC SFDP Task Group authorized by the JC-42.4 Committee Chairman.

The intended audience is serial flash vendors and engineers writing device drivers for SFDP compliant serial flash devices.

The participating SFDP TG members included volunteers from Adesto, Infineon, Giga Device, Intel, ISSI, Macronix, Micron, Microchip, NXP, Sanyo, and Winbond.

Introduction

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors.

The SFDP standard defines a common parameter table describing important device characteristics and serial access methods used to read the parameter table data. Optional Special Function parameter tables for erase sector address map and 4-byte address instructions are included. In the JESD216D revision are optional Special Function parameter tables for the JEDEC x4 (Quad) eXtended Serial Peripheral Interface (x4 xSPI). New in the JESD216E revision is a description of the Replay Protected Monotonic Counter (RPMC) functionality and also descriptions of the Secure Read and Secure Write packet transfer transactions. Additional parameter headers and tables can be specified by future revisions of this standard or by flash vendors and are optional.

SERIAL FLASH DISCOVERABLE PARAMETERS (SFDP) STANDARD

From JEDEC Board Ballot JCB-21-49, formulated under the cognizance of the JC-42.4 Committee on Nonvolatile Memory, item 1775.73.

1 Scope

The SFDP standard defines the structure of the SFDP database within the memory device and methods used to read its data.

The JEDEC-defined header with Parameter ID FF00h and the related Basic Parameter Table is mandatory. This header and table provide basic information for a Serial Peripheral Interface (SPI) protocol memory. Additional headers and tables are optional.

The read command protocol using various I/O modes and standard clock rate are specified. The device electrical parameters are not specified.

2 Normative reference

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents listed. For undated references, the latest edition of the normative document referred to applies.

1. JEP106, *Standard Manufacturers Identification Code* (see www.jedec.org for latest revision)
2. NIST SP800-147, *BIOS Protection Guidelines*
(<http://nvlpubs.nist.gov/nistpubs/Legacy/SP/nistspecialpublication800-147.pdf>)
3. JEDEC Standard JESD251, *eXpanded Serial Peripheral Interface (xSPI) for Non Volatile Memory Devices* as approved by JC42.4 committee in the June 2017 meeting.

JEDEC Standard JESDxxx, *SPI Protocol Reset (Serial Peripheral Interface - Flash Hardware Reset Method, Not Requiring a Dedicated Reset Signal Input)*, **This document is in development.**

4. JEDEC Standard JESD230C, *NAND Flash Interface Interoperability*