JEDEC STANDARD

JEDEC Module Sideband Bus (SidebandBus)

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Contents

Tables

Figures

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JEDEC Module Sideband Bus (SidebandBus)

From JEDEC Board Ballot JCB-21-51, formulated under the cognizance of the JC-45 Committee on DRAM Modules, item 2260.56.

1 Scope

This standard defines the assumptions for the system management bus for next generation memory solutions; covering the interface protocol, use of hub devices, and voltages appropriate to these usages.

2 Terms and definitions

This standard has been updated to utilize terms with preferred social and cultural connotations.

Table 1 — Terminology

Term	Definition
CCC	Common command code.
Controller	A SidebandBus Controller device controls information flow on the I3C Basic bus. It drives the bus clock and coordinates data flow. It provides pull-up voltages on the Host bus data lines.
HID	Host identifier. This 3-bit field uniquely selects one out of up to eight Hub devices on the Host bus. It defines the three least significant bits of the Hub's I3C Basic device address.
Host	SidebandBus/I3C Basic bus Controller.
Host bus	I3C Basic bus between the Controller and Hubs or other I3C Target devices not isolated behind a Hub.
HSA	Host SidebandBus bus device ID address pin; input to a Hub or other Target device to distinguish between identical devices in the I3C Basic address range.
HSCL	Host SidebandBus bus clock, supplied by the Controller.
HSDA	Host SidebandBus data, connected from the Controller to Hubs or Host bus Target devices.
Hub	A SidebandBus Hub is a device that isolates loads on the I3C Basic bus, increasing the number of supported devices on a bus. It provides pull-up voltages on the local bus data lines.
I3C Basic	Serial bus specification defined in coordination with MIPI used as a basis for SidebandBus.
LID	Local identifier. This 4-bit device type identifier uniquely defines one of up to 15 devices on a local bus. It defines the four most significant digits of the local bus device's I3C Basic address.
Local bus	I3C Basic bus between a Hub and Target devices isolated by the Hub from the Host bus.
LSA	Local bus SidebandBus device ID address pin to distinguish between identical devices in the I3C Basic address range.
LSCL	Local SidebandBus clock, driven by the Hub to local bus Target devices.
LSDA	Local SidebandBus data, connected from the Hub to local bus Target devices.
Master	Replaced with "Controller"
PEC	Packet error code.
PMIC	Power management integrated circuit, i.e., voltage regulator.
SA	SidebandBus device ID address pin, generically (Host or Local bus).
SCL	SidebandBus clock, generically (Host or Local bus).
SDA	SidebandBus data, generically (Host or Local bus).
SidebandBus	System management bus for next generation memory solutions, based on I3C Basic.
Slave	Replaced with Target
SPD	Serial Presence Detect Hub device.
Target device	A SidebandBus Target device receives input from a Controller device or as pass-through on a Local bus from a Hub device.