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Guideline to Specify a Transient Off-State Withstand Voltage Robustness Indicator in Datasheets for Lateral GaN Power Conversion Devices, Version 1.0

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Foreword

This document was formulated by JEDEC JC-70.1 GaN Power Electronics Conversion Semiconductor Standards subcommittee consisting of worldwide industry experts from various power semiconductor, metrology, and processing equipment manufacturing companies and users of power semiconductors.

This document is intended for use in the GaN power semiconductor and related power electronic industries and provides guidelines for datasheet parameter specifications for lateral High Electron Mobility Transistors (HEMT) based GaN devices.

Introduction

For the traditional silicon vertical power Field Effect Transistor (FET), the voltage parameter used in a datasheet to specify the maximum voltage that will be blocked (also called withstand or withhold) between drain and source in an off-state is typically the avalanche breakdown voltage. Lateral GaN devices are not yet being built with avalanche capability [1]. Thus, datasheets for lateral GaN devices specify a maximum drain to-source voltage (V_{DS}) that the device will block (or withstand) in an off-state, which is typically much less than the reverse breakdown voltage at which irreversible failure occurs. However, lateral GaN devices exhibit a distinct behavior compared to vertical silicon power FETs, whereby lateral GaN devices can sustain an increased blocking voltage for short durations [2,3,4].

During system design, the concepts of margin and robustness are considered, especially for the occurrence of short over-voltage (or ringing) situations in application. Consequently, this transient blocking voltage can be considered a useful system design parameter for margining purposes and its specification in the datasheet would be beneficial.

The specific details of the breakdown mechanism can vary with different specific lateral HEMT structures. Regardless, the transient nature of the breakdown voltage has been reported in the literature across different lateral GaN processes and structures [6, 7, 8, 9]. Different possible specification techniques for capturing the transient nature of the blocking voltage during off-state are possible. This guideline describes several different specification techniques that are all equally valid for providing a robustness indicator for a transient off-state withstand voltage parameter ($V_{DS(tr)}$) in datasheets. Note that the off-state withstand voltage may not be representative of hard-switching or other types of operation due to the different types of stress applied to the device [5].

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(From JEDEC Board Ballot JCB-21-63, formulated under the cognizance of the JC-70.1 Subcommittee on GaN Power Electronic Conv. Semiconductor Standards.)

1 Scope

This guideline describes different techniques for specifying a Transient Off-state Withstand Voltage Robustness Indicator in datasheets for lateral GaN power conversion devices. This guideline does not convey preferences for any of the specification types presented, nor does the guideline address formatting of datasheets. This guideline does not indicate nor require that the datasheet parameters are used in production tests, nor specify how the values were obtained.

This guideline is not intended to provide a methodology to convert between the different specification types, nor imply any of the robustness indicators in this guideline are used to calculate lifetimes. This guideline is not meant to imply the robustness indicators are for unlimited pulses or cycle-by-cycle transient withstand voltage excursions. This guideline applies only to off-state, and does not apply to other operating modes, such as hard switching, which may place a different type of stress on the device.

However, this guideline does not preclude the specification of a transient withstand voltage for unlimited pulses or cycle-by-cycle. This guideline also does not preclude specifying a transient voltage for other operating modes, such as hard switching or input surge operation. This guideline also does not prevent having a transient voltage parameter on a datasheet which is tied to detailed lifetime and reliability models.

2 Terms, definitions and letter symbols

V_{DS}	drain to source voltage of DUT
$V_{DS(off)}$	drain to source voltage of DUT, in Off state
$V_{DS(tr)}$	transient blocking drain to source voltage

3 $V_{DS(tr)}$ Specification Options

3.1 Transient Specification Traits

Different techniques (or types or methods) for specifying the transient nature are acceptable. The key guideline for any method is it possesses the following traits in its specification:

1) Maximum transient drain-source blocking voltage,
2) a pulse width in time or damping time,
3) number of pulses, damping time behavior, or imply rare event or atypical occurrence, and
4) temperature.